CHAMELEON: ULP* MCU SUBSYSTEM

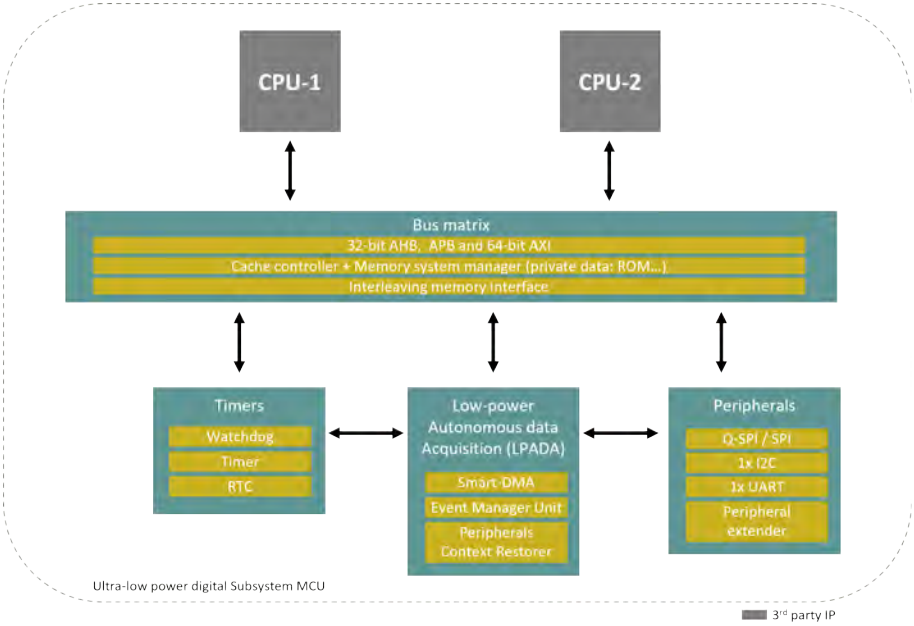
WHAT IS CHAMELEON?

The Chameleon MCU Subsystem, is a versatile and open IP platform configurable for single or dual-core processors. Designed for smart devices, this scalable subsystem enhances energy efficiency in SoCs. It supports intelligent data and device management, allowing devices to function independently of a CPU. Key features include a standalone autonomous Smart-DMA, a fine-grained power management unit, a low-latency interconnect, and an event manager. Initially pre-instantiated for Cortex M, it can be adapted for other cores, such as Risc-V. Additionally, the subsystem seamlessly integrates with Dolphin Design's SPIDER power management platform, ensuring full interoperability.

APPLICATIONS

- Internet of Things (IoT)
  WiFi, BLE, Cellular
- Beacons
- Wearables
- Computer peripherals and IO devices
- Low-power intelligent devices
- Real time industrial application

Chameleon IP block diagram



Key features

- Arm and Risc-V CPU supported
- 32- bit AHB 3.0 Bus Channel / Decode
- 32-bit APB 3.0 Bus Channel /decide
- AHB to APB bridge
- 64-bit AXI Lite 4.0
- Autonomous peripheral

Deliverables

- System Verilog RTL code
- Acceptance test bench (and tests)
- Test bench with test suites
- User manuals (integration, programming)
- CMSIS Low-level HW Drivers
- FreeRTOS (ported examples)
- Virtual platform (TLM design view)

DOLPHIN DESIGN