

## DOLPHIN DESIGN EMPOWERS YOUR CREATIVITY

Dolphin Design is a leading provider of semiconductor IP solutions, specializing in ASIC and IP design targeting markets such as Defense, Automotive, Industrial, Personal electronics and IoT. Dolphin Design's cutting-edge technology IPs in AI computing, Power management, High-quality Audio, Power metering and Design Safety/robustness, allows their thousand customers and partners to accelerates design cycles, fosters faster time-to-market and builds products/solutions that address the challenges of any industries and support a more sustainable world.

# DOLPHIN

DESIGN

## YOUR SALES INTERFACES

### China

**Ying ZHAO**  
+33 476 417 425  
ying.zhao@dolphin.fr

### Americas

**Ranjit ADHIKARY**  
+1 408 515 5870  
ranjit.adhikary@dolphin.fr

### EMEA

**Romain Chantre**  
+33 7 50 59 68 34  
romain.chantre@dolphin.fr

# IP SOLUTIONS CATALOG

H1 - 2024

**DOLPHIN**  
DESIGN

**Dolphin Design**  
1 bis A, Chemin du Pré Carré,  
38240 Meylan  
dolphin-design.fr  
+33 4 76 41 10 96



SCAN TO CATALOGUE

# TECHNOLOGICAL INNOVATION IS OUR JOURNEY

At Dolphin Design, we believe that it is possible to reconcile long-term sustainability with technological innovations that contribute to make our life better.


Our contribution, to make this happen, is to design silicon IPs enabling the cost-effective design of highly energy-efficient and ever more complex ASIC/SOCs, either made by, or for our clients.

We pave the way for intelligent SoCs that will ultimately operate with green energy or with harvested energy.


We tech it on!




## Advanced Processing Solutions Computer Vision, DSP, and MCU Subsystem Platform IPs

NN accelerator IP platform - RAPTOR 					Digital IP
	MACs	MAC efficiency	DMA	Supported layers	SDK compliance
Neural accelerator	32	Up to 60%	Yes	CNN	Pytorch, TensorFlow
	64				
	128				

NN/DSP co-processor IP platform - PANTHER 					Digital IP
	# DSP cores (# MACs)	RISC-V compliance	DMA	Floating Point Unit (FPU)	SDK compliance
Neural/DSP co-processor	4 DSP cores (4x 32-bit MACs 8x 16-bit MACs 16x 8-bit MACs)	IMCF + X	Yes	Yes (32 bits)	C-based SDK (including C-Compiler...) AI SDK (soon) for Pytorch and TensorFlow
	8 DSP cores (8x 32-bit MACs 16x 16-bit MACs 32x 8-bit MACs)	IMCF + X	Yes	Yes (32 bits)	C-based SDK (including C-Compiler...) AI SDK (soon) for Pytorch and TensorFlow
	16 DSP cores (18x 32-bit MACs 32x 16-bit MACs 64x 8-bit MACs)	IMCF + X	Yes	Yes (32 bits)	C-based SDK (including C-Compiler...) AI SDK (soon) for Pytorch and TensorFlow

IP subsystem platform - CHAMELEON 				Digital IP
	Supported CPUs	Supported protocols	Built-in features	Built-in peripherals
Single core	ARM Cortex M & RISC-V	AMBA - AHB, AXI, APB	Multi-channel bi-directional DMA, DMA filter, Event Unit Manager, Context restorer, low-latency multi-master bus matrix with built-in interleaving engine	Communication: UART, I2C master, QSPI master, OctoSPI master Others: GPIO, GP Timer, Advanced Timer, Watchdog timer...
Dual core	ARM Cortex M & RISC-V (including hw semaphore for parallel processing)	AMBA - AHB, AXI, APB	Multi-channel bi-directional DMA, DMA filter, Event Unit Manager, Context restorer, low-latency multi-master bus matrix with built-in interleaving engine	Communication: UART, I2C master, QSPI master, OctoSPI master Others: GPIO, GP Timer, Advanced Timer, Watchdog timer...



# SPIDER IPs - State-of-the art solution for Power Management

As a three-decade leader in Power Management IP, we've tailored solutions to fit your exact design needs, saving you time and resources while accelerating your time-to-market and boosting design productivity.

Power management IP platform					180nm	55nm	40	22nm	12nm Roadmap 2024	
	V <sub>IN</sub> (V)	V <sub>OUT</sub> (V)	I <sub>OUT</sub>	I <sub>Q</sub> (µA)						
DC/DC Buck	Single input, multiple outputs SIMO DC/DC - Low quiescent	[1.8 - 5.5]	[0.5 - 3.5]	Up to 400 mA	0.64 to 1.5 µA				✓	0
	Single input, single output DC/DC - Low quiescent	[1.62 - 5.5]	[0.5 - 3.3]	100 mA - 1 A	0.35 to 0.37 µA				✓	0
		[1.62 - 3.63]	[0.5 - 2.5]		0.29 to 0.37 µA				✓	
	DC/DC - Mainstream	[1.9 - 5.5]	[0.5 - 3.3]	100 mA - 1 A	80 to 100 µA				✓	
		[2.7 - 5.5]	[0.55 - 3.3]		130 to 187 µA				✓	
	DC/DC - Legacy	[1.62 - 3.63]	[0.6 - 3.3]	100 mA - 1 A	75 to 100 µA	✓	✓	✓	✓	
[1.9 - 4.4]		[0.6 - 3.3]	100 mA - 700 mA	70 to 125 µA	✓	✓				
Combo DC/DC Mainstream DC/DC + Low quiescent LDO	[1.9 - 5.5]	[0.5 - 3.3]	100 mA - 1 A	(sleep) = 0.25 to 0.6 µA (active) = 100 to 130 µA				✓		
	[2.7 - 5.5]	[0.55 - 3.3]		(sleep) = 0.37 µA // (active) = 155 µA				✓		
	[1.62 - 3.63]	[0.55 - 3.3]		100 mA - 700 mA	(sleep) = 0.14 to 0.37 µA (active) = 75 to 100 µA	✓	✓	✓	✓	
LDO - Fast transient	[1.8 - 5.5]	[0.5 - 3.3]	100 mA - 500 mA	25 to 65 µA				✓	0	
	[2.7 - 5.5]	[0.55 - 3.3]		40 to 125 µA	✓			✓		
	[1.44 - 1.98]	[0.6 - 1.2]		40 µA				✓		
	[1.62 - 3.63]	[0.6 - 2.5]		23 to 200 µA		✓	✓	✓		
LDO	[2.7 - 5.5]	[0.55 - 3.3]	up to 1 mA	0.37 µA				✓		
	[1.9 - 4.4]	[0.55 - 3.3]	up to 1 mA	0.075 to 0.17 µA	✓	✓				
	[1.62 - 3.63]	[0.5 - 3.3]	up to 2 mA	0.14 to 0.37 µA	✓	✓	✓	✓	0	
LDO - Capless	[0.72 - 1.8]	[0.5 - 0.9]	up to 50 mA	7.5 to 12 µA				✓	0	
Combo LDO LDO + Low quiescent LDO	[2.7 - 5.5]	[0.5 - 2.5]	100 mA - 500 mA	(sleep) = 0.37 µA - (active) = 40 µA				✓		
	[1.62 - 3.63]	[0.55 - 2.5]		(sleep) = 0.14 to 0.16 µA (active) = 45 to 75 µA		✓		✓		
Oscillators	32 kHz Crystal	[0.72 - 0.99]	Freq = 32.768 kHz	I <sub>Q</sub> = 97 to 165 nA - CL = 4 to 12.5 pF Accuracy = ±50 ppm				✓	0	
		[0.81 - 1.21]		I <sub>Q</sub> = 50 to 120 nA // CL = 4 to 7 pF // Accuracy = ±50 ppm			✓	✓		
	32 kHz RC	[0.54 - 0.99]		I <sub>Q</sub> = 55 to 70 nA Accuracy (after trimming) = ±1.5%				✓	0	
	[0.495 - 1.21]		I <sub>Q</sub> = 70 to 420 nA // Accuracy (after trimming) = ±1.5%		✓	✓				
Monitors	POR-BOR	[1.62 - 3.63]	Monitored (V) = [0-AVD]	13 to 15 µA (continuous operation) < 150 nA (burst operation) < 100 nA (BOR disabled)		✓	✓	✓	0	
		[1.44 - 1.98]		16 µA (continuous operation) < 150 nA (burst operation) < 100 nA (BOR disabled)				✓		
RTC (full digital)	Core voltage			Accuracy = -2.1 to 1.6 ppm Nominal freq: 32.768 kHz	✓	✓	✓	✓	0	
PMU	Adaptive Body Bias							✓		
	Power Controller compiler	GUI-based power controller compiler (RTL & C-drivers) - Boot & power sequences			✓	✓	✓	✓	0	
		GUI-based UPF backbone generator			✓	✓	✓	✓	0	

Low quiescent = Low quiescent

0 = roadmap



# BAT IPs - Amplifying Audio Excellence

For over 30 years, Dolphin Design is leading Audio premium IPs, catering to diverse applications including TWS, Smart speakers, Wearables, IoT, Automotive, and more. Our BAT IP family offers seamless configurability and assembly for high-fidelity, low-power audio devices, ensuring faster time-to-market with robust and advanced IPs.

Mixed signal Voice & Audio IP platform						180nm	55nm	40nm	28nm	22nm	12nm
	Power supply	SNR	THD+N	Input noise	Power consumption						
ΔΣ 24-bit ADC(*)	Voice/audio ADC - Performance	1.8 V +/- 10%	107 dB	-98 dB	3.1 µVrms	Full perf. mode: 250 µA Low power mode: 125 µA				0	0
	Voice/audio ADC - Mainstream+	1.8 V +/- 10%	104.5 dB	-75 dB	2.6 µVrms	Full perf. mode: 550 µA Low power mode: 150 µA				✓	✓
		1.8 V to 3.3 V	109 dB	-75 dB	2.6 µVrms	Full perf. mode: 550 µA Low power mode: 150 µA			✓		
	Voice/audio ADC - Mainstream	1.8 V +/- 10%	101 dB	-80 dB	3.8 µVrms	Full perf. mode: 550 µA Low power mode: 170 µA				✓	✓
		1.8 V to 3.3 V	106 dB	-80 dB	3.8 µVrms	Full perf. mode: 550 µA Low power mode: 140 µA			✓		
Voice/audio ADC - Legacy	2.7 V to 3.63 V	90 dB	-90 dB	7.7 µVrms	Full perf. mode: 1.7 mA		✓	✓			
	1.8 V +/- 10%	85 dB	-80 dB	8 µVrms	Full perf. mode: 1.7 mA				✓	✓	
(*) provided stand-alone or as part of CODEC configuration											
	Power supply	SNR	THD+N	Output noise	Power consumption						
ΣΔ 24-bit DAC(*)	Audio DAC + class-D amp. - performance	1.8 V +/- 10%	115 dB	-95 dB	1.78 µVrms	915 µA without load 1.055 mA at 0.1 mW				0	✓
	Audio DAC + class-AB amp. - Mainstream	1.8 V +/- 10%	115 dB	-90 dB	1.9 µVrms	1,175 µA without load 3.4 mA at 0.1 mW				✓	
		1.8 V to 3.3 V	120 dB	-90 dB	1.9 µVrms	1,175 µA without load 3.4 mA at 0.1 mW				✓	
Audio DAC + class-AB amp. - Legacy	2.97 V to 3.63 V	100 dB	-90 dB	6 µVrms	2,200 µA without load		✓	✓			
0 = roadmap											
Smart audio IP platform						180nm	55nm	40nm	28nm	22nm	12nm
	Input signal	Output signal	Main clock	Power consumption							
VUI	Voice Activity Detection WhisperTrigger	Analog microphone	IRQ upon voice detection	32 kHz RC or 32 kHz crystal	13 µW @ 40 & 22nm		✓	✓		✓	
		Digital microphone	IRQ upon voice detection	From 6 MHz to 13 MHz	25 µW @ 40 nm	✓	✓	✓	✓	✓	✓
	Audio neuromorphic front end (aMFCC) WhisperExtractor	Analog microphone	MFCC data IRQ upon voice detection	32 kHz RC or 32 kHz crystal	7 µW @ 22 nm			0		✓	0
0 = roadmap											
Digital Audio IP platform						Phase alignment	PLL less filters	Low latency filters	Asynchronous interface		
	SNR	THD+N	Main clock	Number of channels							
Digital audio	PDM to PCM converter Digital microphone input	117 dB	-110 dB	12 or 11 MHz or 19.2 MHz 12.288 MHz or 11.2896 MHz	From 1 to 8	✓	✓	✓		✓	
	Digital audio DAC PWM	110 dB	-95 dB	12 or 11 MHz or 19.2 MHz 12.288 MHz or 11.2896 MHz	From 1 to 8	✓	✓		✓		✓
	Asynchronous Sample Rate Converter ASRC	114 dB	-114 dB	24 or 26 MHz or 24.576 MHz	From 2 to 8	✓	✓		✓		✓

Phase alignment: Ensure 0° phase mismatch between channels for accurate beamforming.

PLL-less: Use standart clock available in your system and save an audio PLL.

Low latency filters: Enable µs latency for applications like ANC or RNC.