DOLPHIN

DESIGN

POWER MANAGEMENT TOTAL SOLUTION TO ENABLE THE FASTEST AND SAFEST DESIGN OF ENERGY EFFICIENT AIOT SOCS

SAFE FORUM

October 17, 2019

Frederic Renoux – EVP Sales

FABLESS QUEST FOR ENERGY-EFFCIENCY

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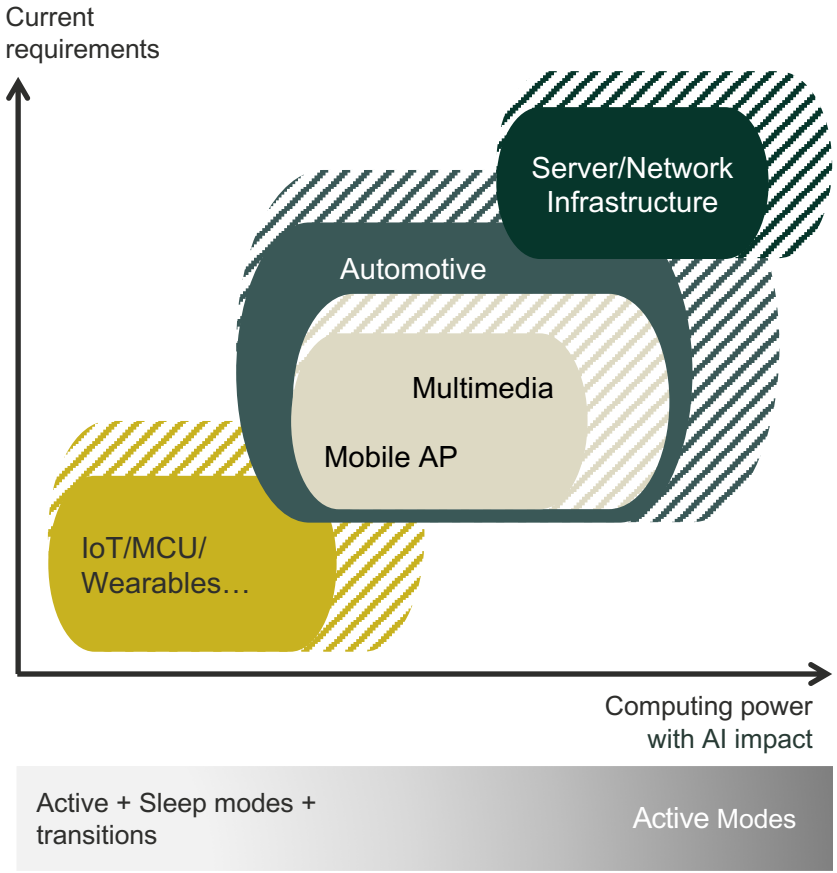
AIoT A CONCENTRATE OF ENERGY EFFICIENCY CHALLENGES

"*One of today's technology most significant challenges is how to create a SOC that meets the conflicting consumer demand for devices with both* ***high performance*** *and* ***extended battery life***"

Samsung Semiconductor business

« *…**Power management** is another feature, which in some cases may be the **determining factor** for whether a product (MCU) does well or fails because it affects battery life. Some of these MCUs have more than 16 low-power states, but to transition from one power state to the next is complex.* »

Andrew Caples, Mentor a Siemens business



RECIPES TO IMPROVE ENERGY-EFFICIENCY OF AIoT

PROCESS NODE

LP DESIGN TECHNIQUES

SoC ARCHITECTURE

RECIPES TO IMPROVE ENERGY-EFFICIENCY OF AIoT

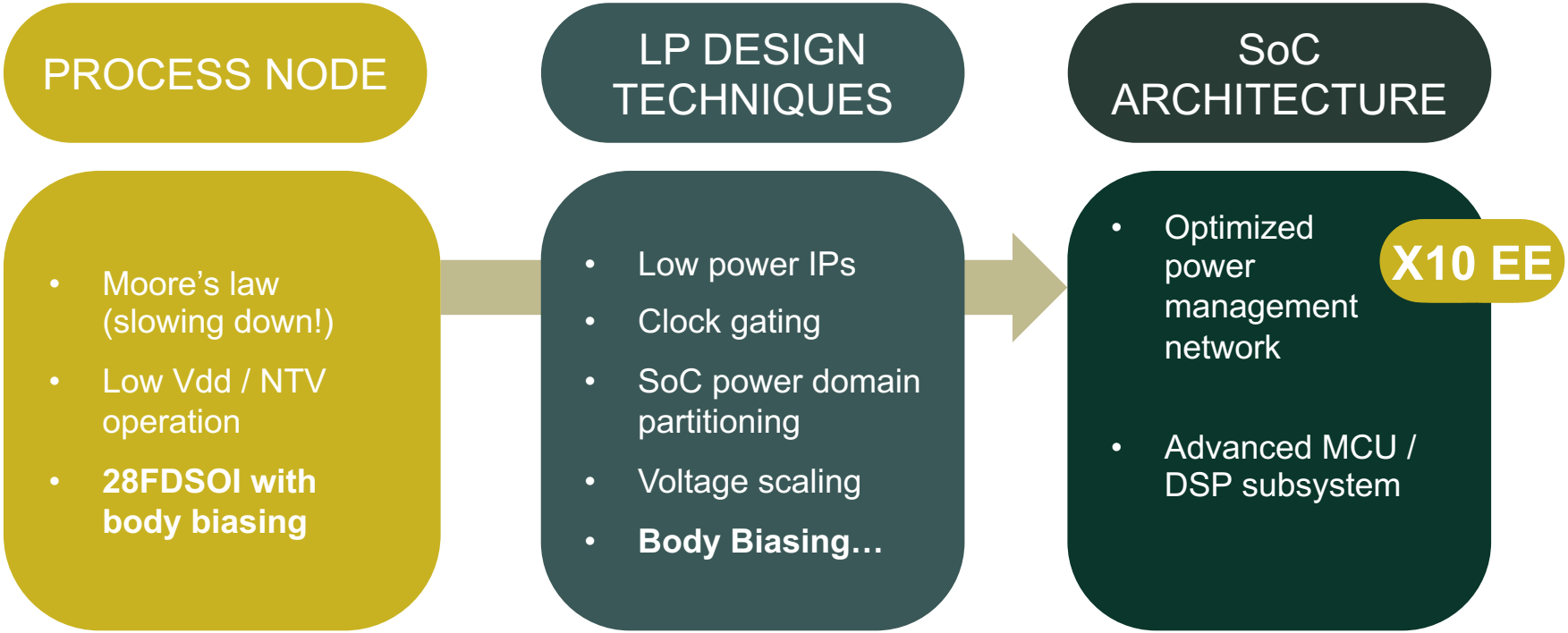
PROCESS NODE

- Moore's law (slowing down!)
- Low Vdd / NTV operation
- **28FDSOI with body biasing**

Some of key selection factors of 28FDS

- **Ultra Low Voltage** operation thanks to body biasing (down to 0.5V)
- Superior EE in each power mode through **body biasing adjustment**
- **Superior RF** characteristics
  - Still room for improvement with Body Biasing
- **Mask cost** advantage
- **MRAM** maturity…

RECIPES TO IMPROVE ENERGY-EFFICIENCY OF AIoT



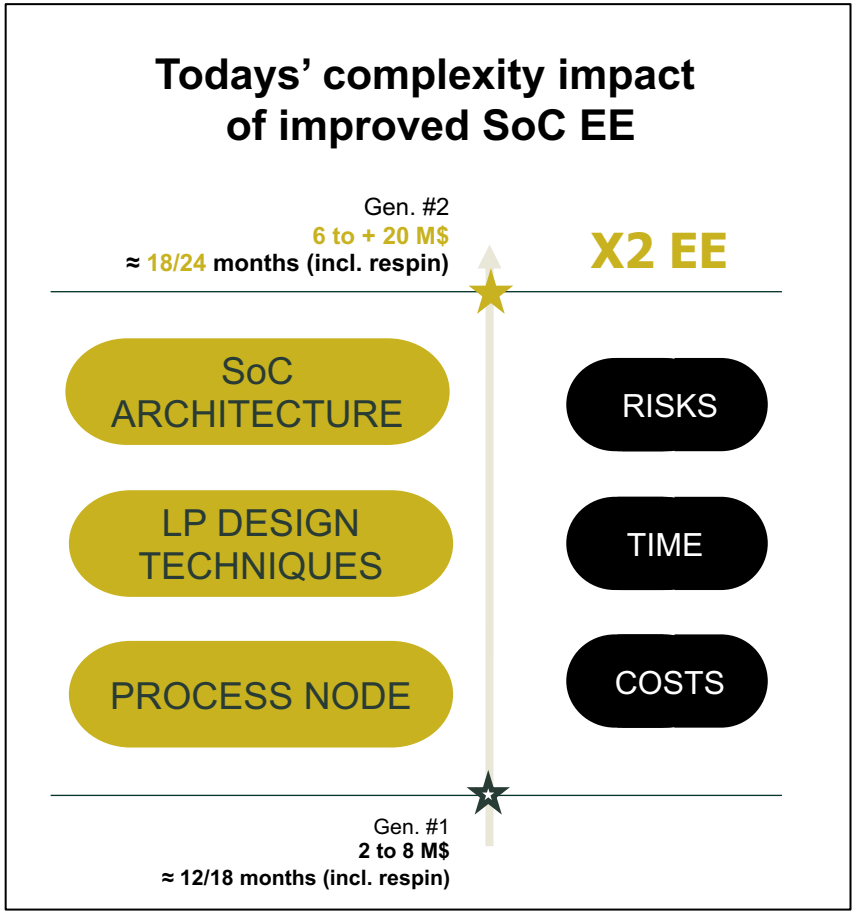
NEEDS ARE HERE (COMPETITIVE), RECIPES ARE KNOWN... SO WHAT?

« The IoT technology market is expected to grow from USD 176.00 Billion in 2016 to USD 639.74 Billion by 2022, at a CAGR of 25.1% during the forecast period. »

Markets and Trends

Last year, 32-bit **ASPs dropped 15%**. "We're seeing 32-bit **prices falling 7% per year (CAGR). It will reach a point** where 32-bit microcontrollers are priced lower than 16-bit microcontrollers. This is pure competition and pricing pressure. IoT is part of the driving force for this.

Rob Lineback, IC Insights



BOTTLENECKS TO YOUR POWER MANAGEMENT CREATIVITY

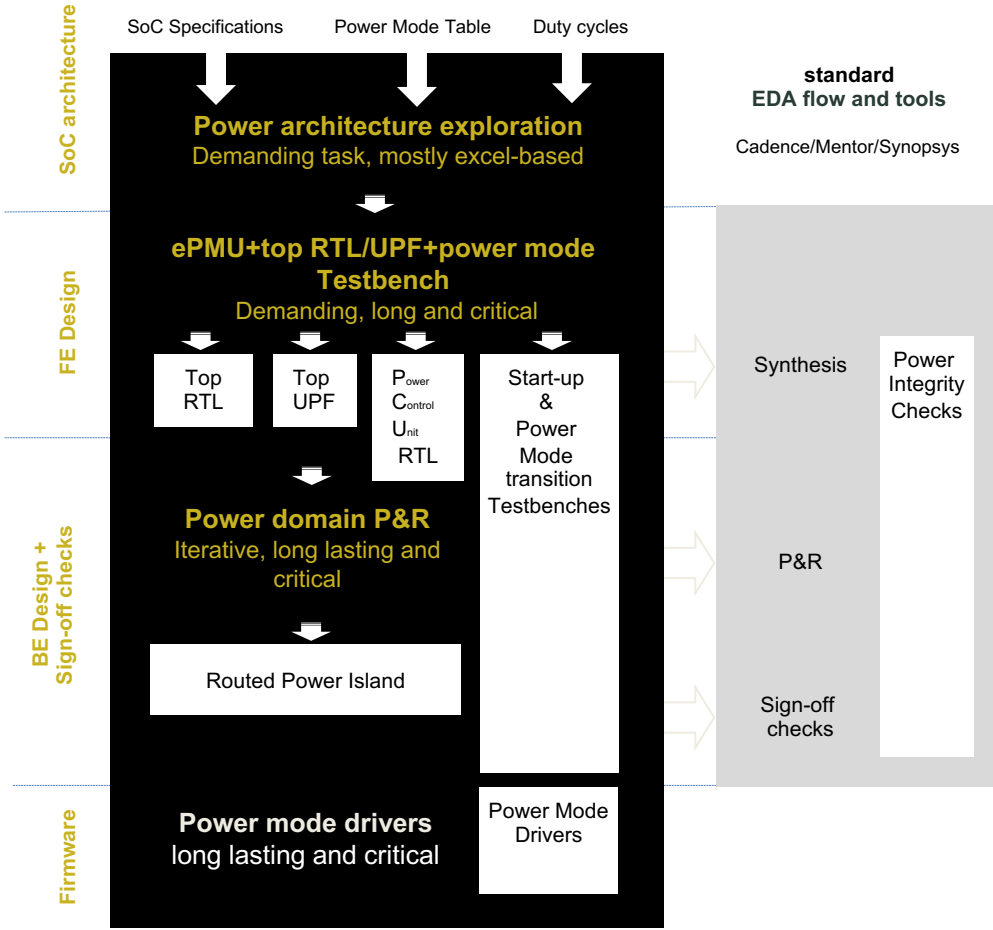
RISKS TIME COSTS

- Complexity of power management implementation prevents companies to leverage advanced LP techniques
  → **Opportunity for improved Energy Efficiency**

- Risks of of performance drops or functionality issues:
  - Start-up/power-up
  - Power mode transition
  - Power integrity, noise impact…

  → **Opportunity for cost savings and faster TTM**

Power management design flow



PAVING THE WAY TO ENERGY-EFFICIENCY WITHOUT LIMITS IN 28FDS

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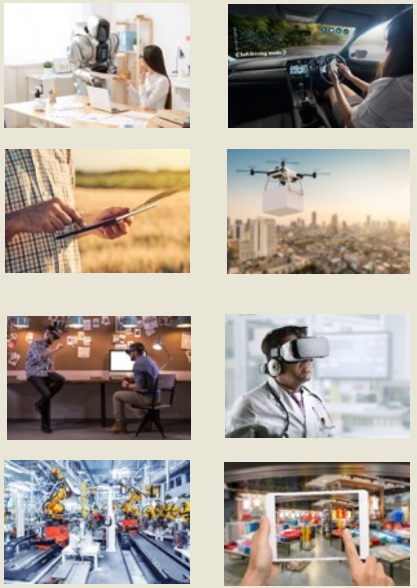
SPEED PM FOR AIoT:

ENERGY-EFFICIENCY WITHOUT LIMITS!

System Platform for EE Designs - Power Management

EDGE APPLICATIONS



SPEED
Power Management

Pre-configured & **Qualified** Power Mgnt IP Cluster (**incl. BB**)

Guided exploration & selection of most EE power architecture

Automated design and implementation of Power Mgnt subsystem

Best Energy Efficiency — **Up to X10**

Lowered System Costs — **Up to x10 cts saved**

Improved Time-To-Success — **Up to 6 months saved**

Lowered Risks — **First Pass Success**

REVOLUTIONIZING THE DESIGN OF EE SOCS IN 28FDS

SPEED
Power Management

Pre-configured & **Qualified** Power Mgnt IP cluster (**incl. BB**)

Guided exploration & selection of most EE power architecture

Automated design and implementation of Power Mgnt subsystem

Faster exploration and selection

Reduced FE design effort

Reduced BE effort

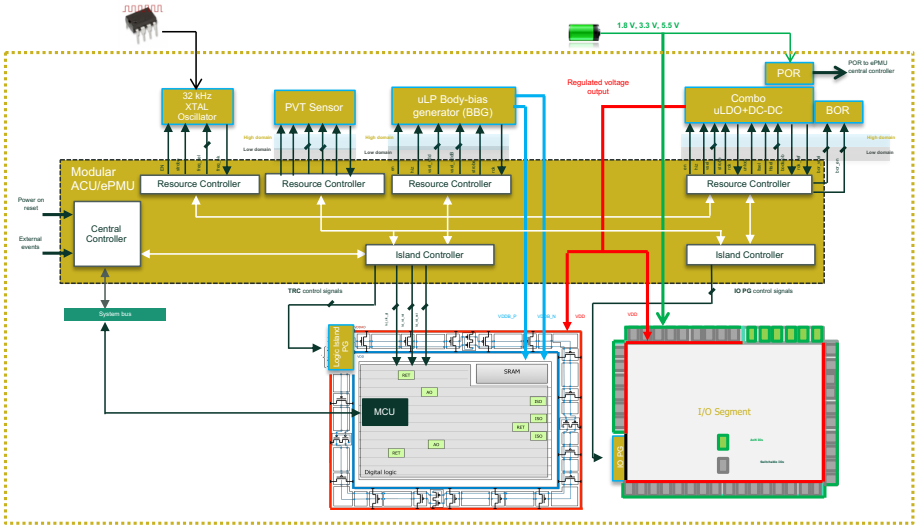
Streamlined power integrity checks

Reduced firmware development effort

BB PDP AVS uLV DVFS

Cadence/Mentor/Synopsys flow

COMPLETE, TAILORED AND SCALABLE CLUSTER OF POWER MANAGEMENT IPs



Leveraging **28FDS** specifics:

- **Ultra-low voltage** enablement with **best speed**
- **Improved RF performances** with Body Biasing enablement (closed loop)

Voltage Regulators (LDO/DC-DC/Combo)

Power Gating (Core/IO)

Body Biasing (Closed loop)

Voltage Monitors (POR/BOR)

Voltage Domain Interfacing cells (LS/ISO/ESD prot.)

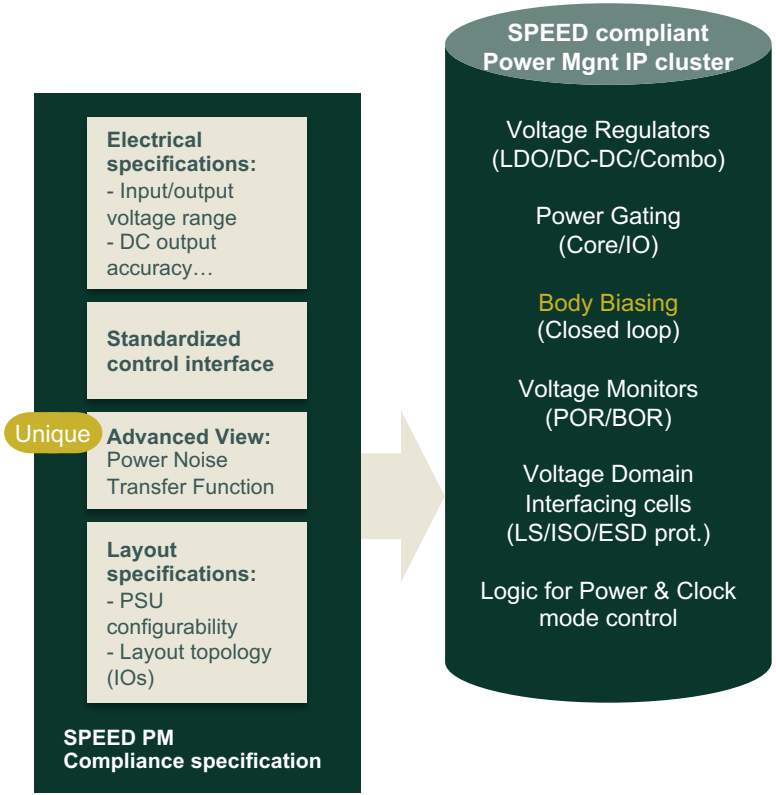
Logic for Power & Clock mode control

POWER MANAGEMENT IP CLUSTER
SPEED PM COMPLIANT

Unified IP specifications
- Secured path to a faster success…

Unified IP deliverables
- To speed-up Time-to-Success

Modular power management construct
- To gain in flexibility & costs



SOC-LEVEL PM OPTIMIZATION TO UNLEASH YOUR CREATIVITY

Best Energy Efficiency at SoC level

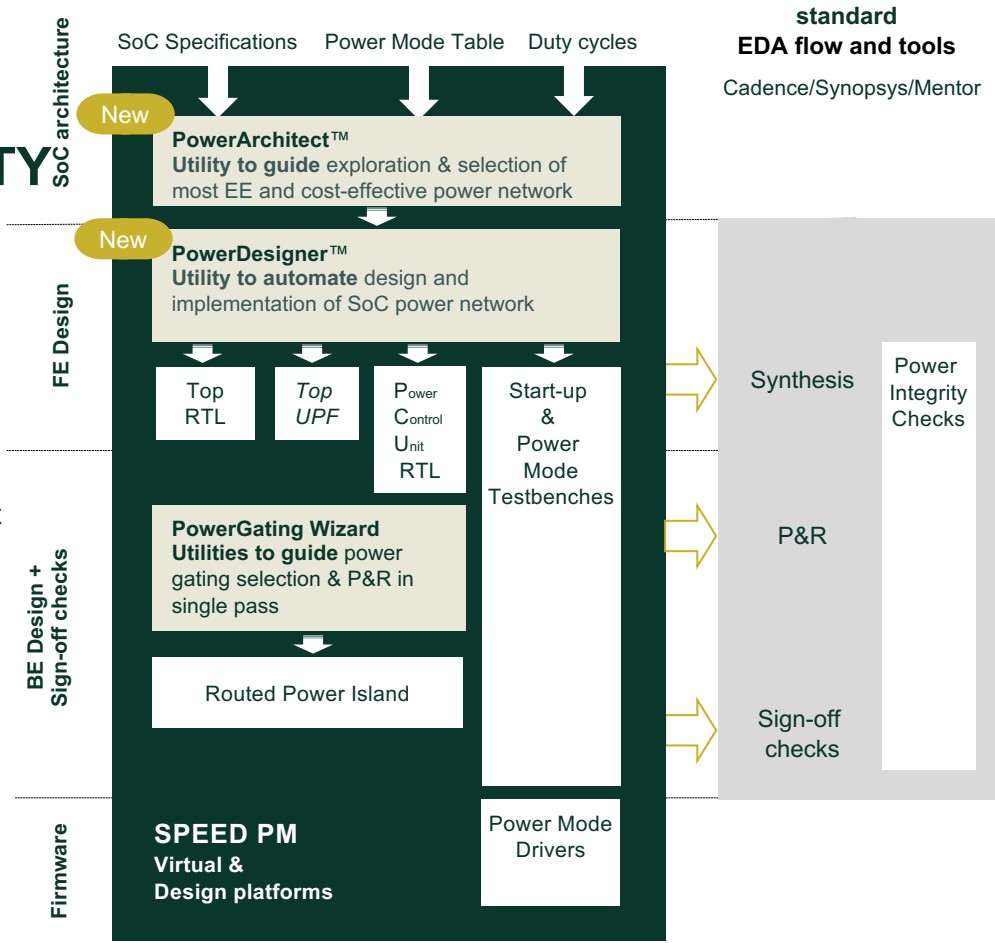
Lowered System Costs

Improved Time to Success

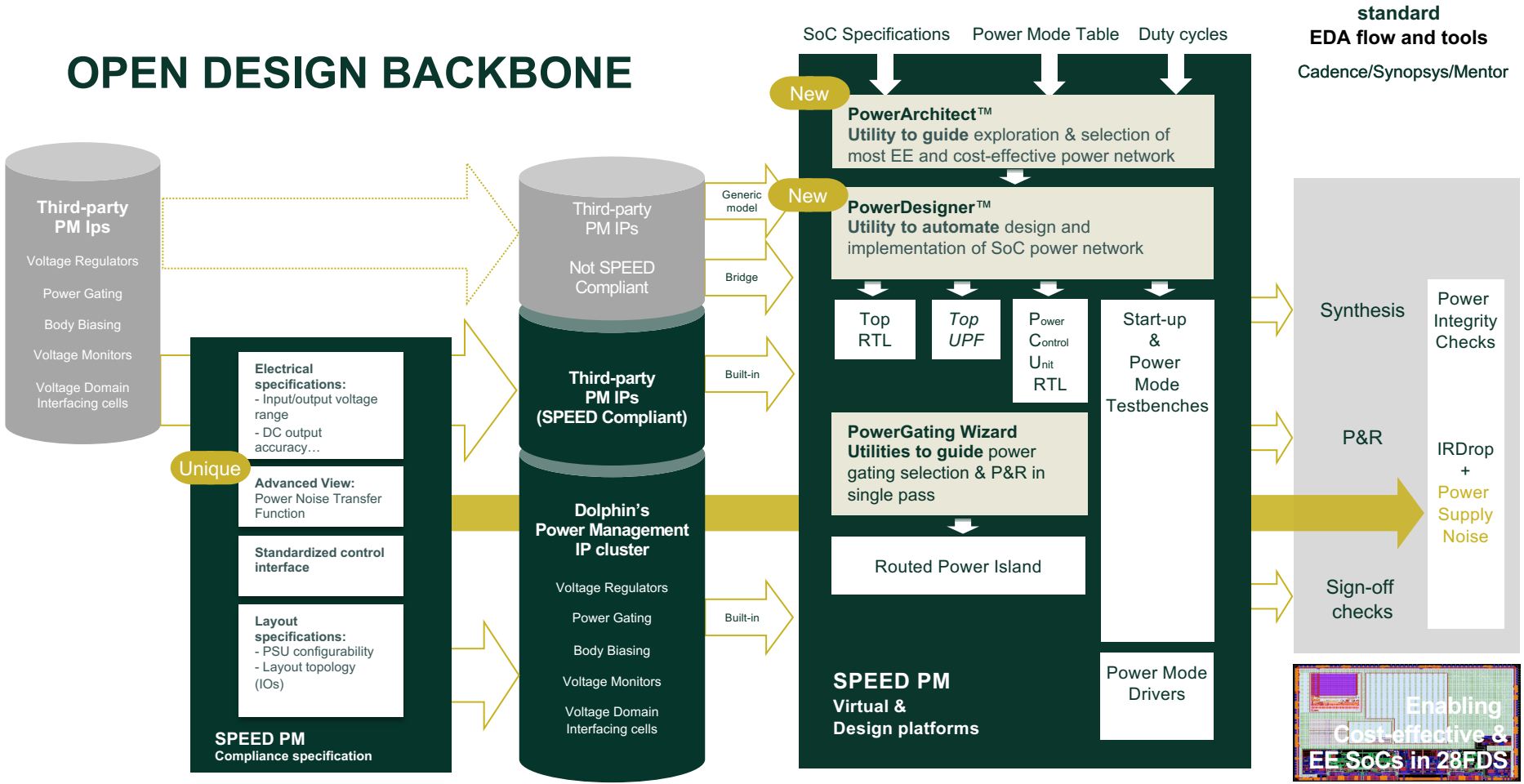
- GUI-based power management network construct
- Automated generation of Top RTL, Power Control Unit, *UPF*
- Consistency checks from power architecture definition…

Lowered risks

- Secured boot/start-up and safe mode transition
- Automated generation of power mode sequence testbench
- ePMU good by construction…



OPEN DESIGN BACKBONE



A JOURNEY TO ENERGY-EFFICIENCY

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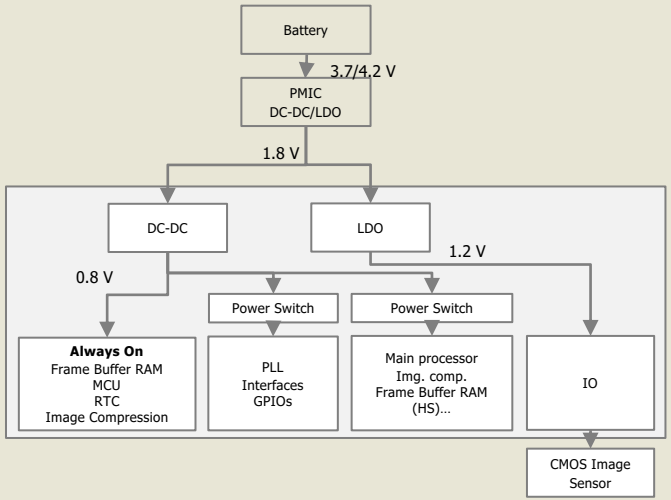
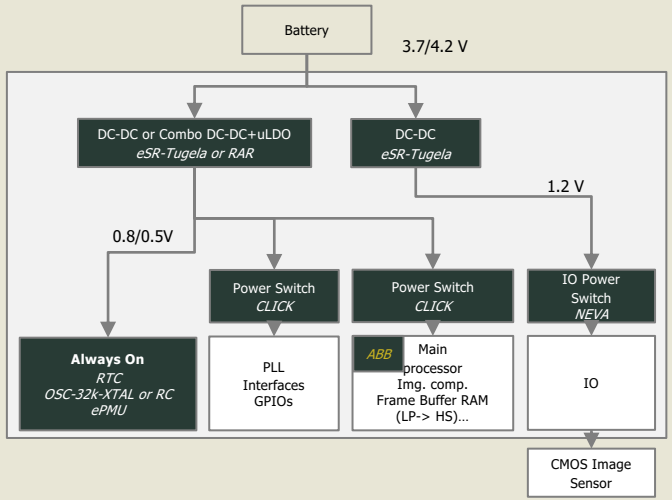
E.G. MAKING A MORE COST-EFFECTIVE & MORE EE ISP IN 28FDS





- **Direct connection to battery** using innovative DC-DC converter designed for high-voltage support
- CMOS Sensor supplied by an **ultra-low noise** and **high-efficiency DC-DC converter**
- **No replication of Frame Buffer RAM nor Image compression block** applying DVFS and ABB on main processor island

- Significant area reduction: **several mm2 saved**
- Energy Efficiency improvement at system level: **up to x10 better EE**
- TTM and BoM cost reduction: **up to $ x10cts saved & weeks of TTM**
- **Reduced PCB area**
- Reduced heat: **less random noise impacting video quality…**

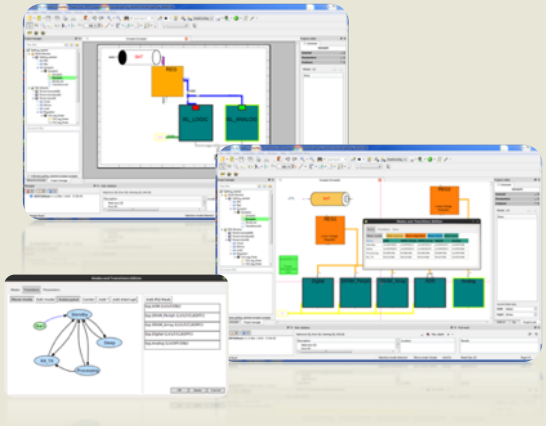
POWER MANAGEMENT PLATFORM

Define & Optimize ISP SoC Power Network

1

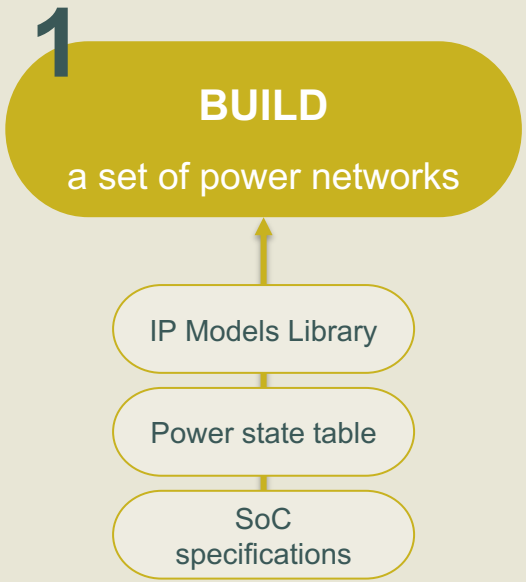
BUILD

a set of power networks



POWER MANAGEMENT PLATFORM

Define & Optimize ISP SoC Power Network



POWER MANAGEMENT PLATFORM

Define & Optimize ISP SoC Power Network

1

BUILD

a set of power networks

- IP Models Library
- Power state table
- SoC specifications

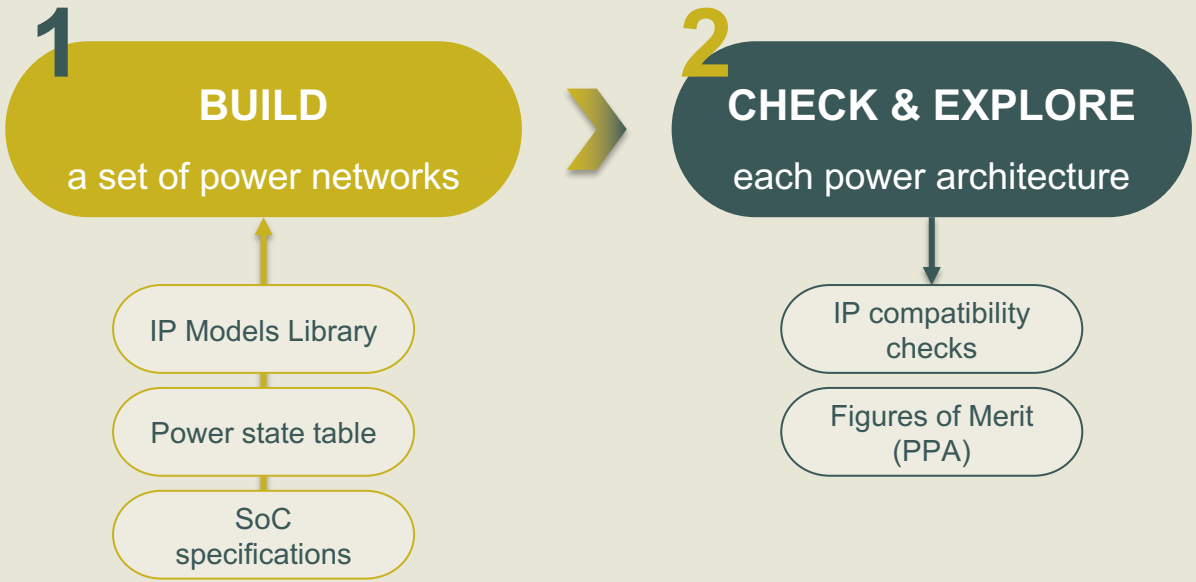
2

CHECK & EXPLORE

each power architecture

POWER MANAGEMENT PLATFORM

Define & Optimize ISP SoC Power Network



POWER MANAGEMENT PLATFORM

Automate SoC Power Network design and implementation

1 BUILD
a set of power networks

- IP Models Library
- Power state table
- SoC specifications

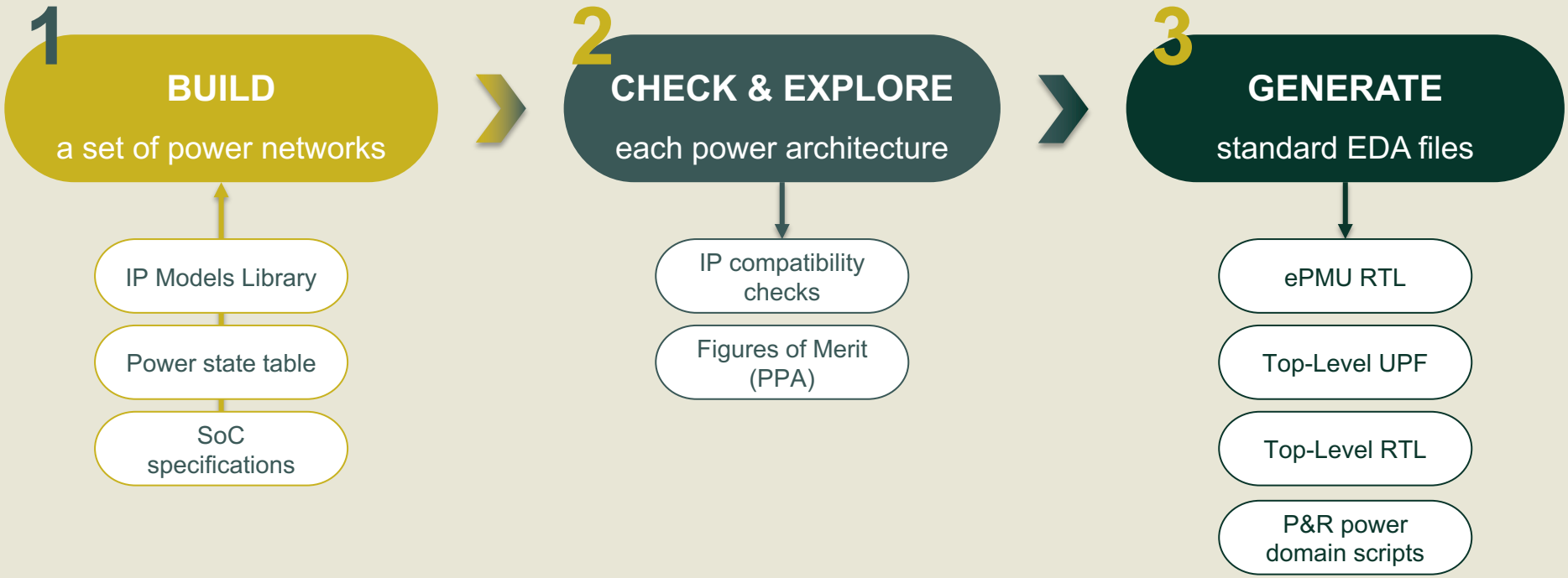
2 CHECK & EXPLORE
each power architecture

- IP compatibility checks
- Figures of Merit (PPA)

3 GENERATE
standard EDA files

POWER MANAGEMENT PLATFORM

Automate SoC Power Network design and implementation



TAKE-AWAY:
WHY CONSIDERING SPEED PM IN 28FDS?

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AIoT LOOKING FORWARD IN 28FDS

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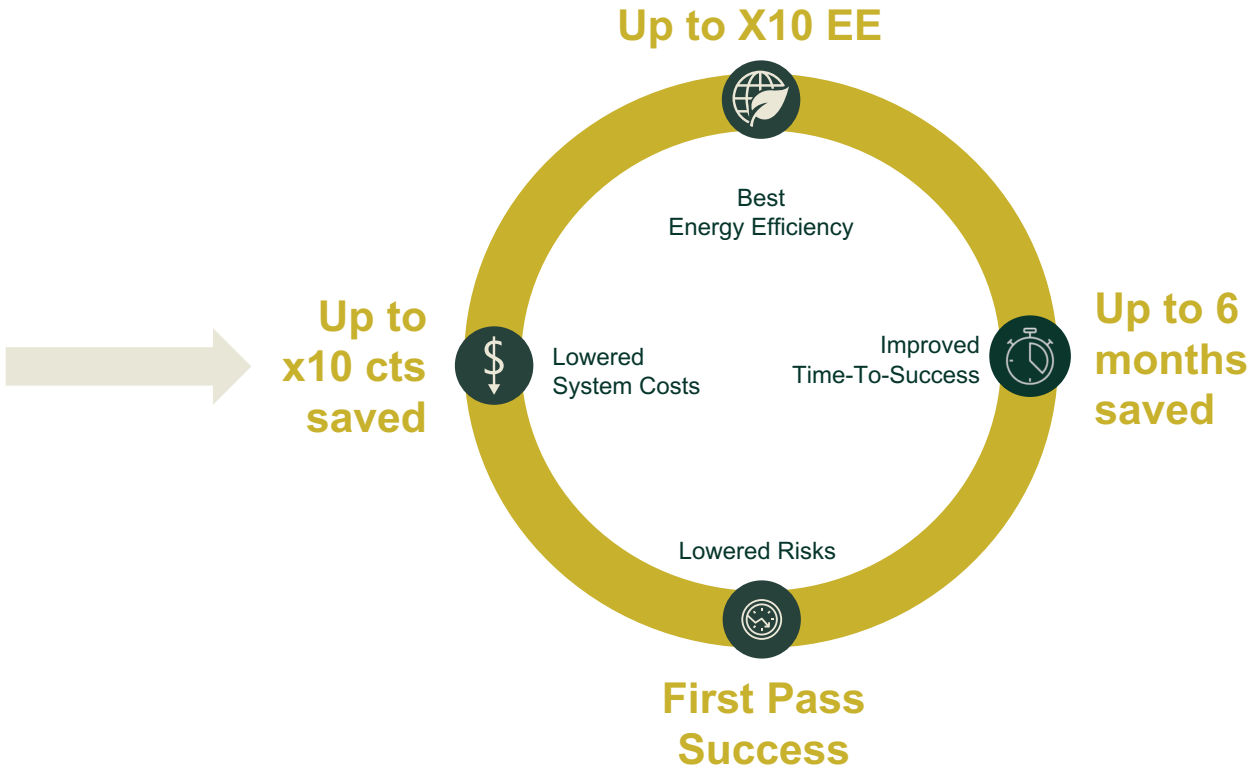


UNLEASH YOUR CREATIVITY TO EMPOWER YOUR MARKET IMPACT

Enhanced competitive advantage = **more market share**

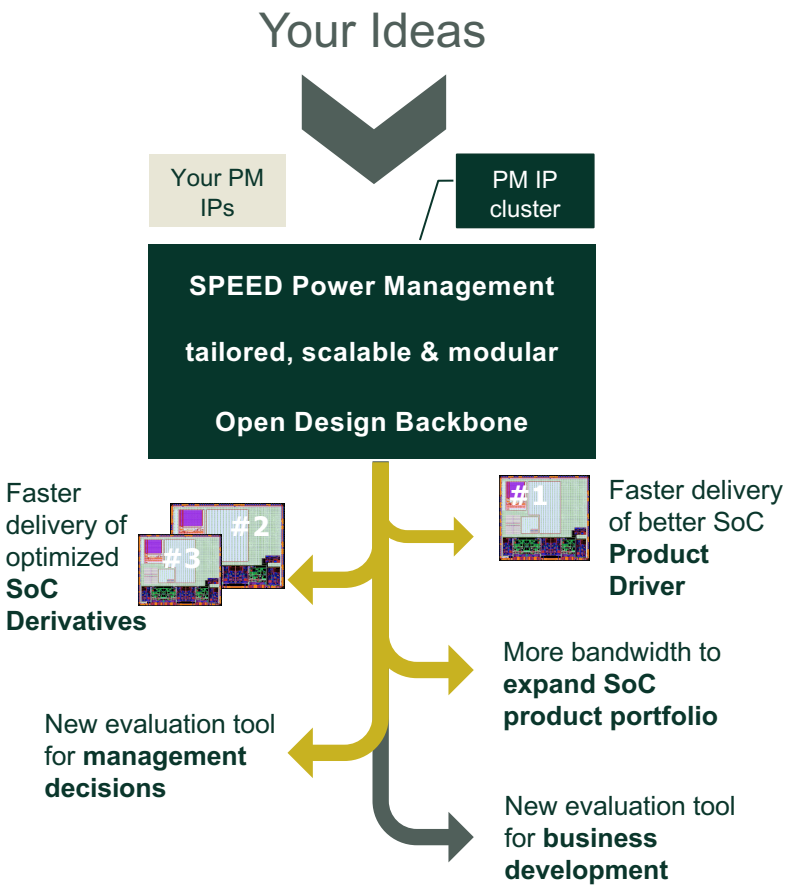
- SoC-level PPA optimization

Faster Time-To-Success = **improved cost-structure**

- Reduced design efforts and reduced risks of respin translate into reduced unit costs

Scaled design activity = **revenue growth**

- Do more with same engineering resources
- SPEED PM can apply to any process and application to reach faster and more cost-effectively new market segments



FUTURE COLLABORATIONS PLAN WITH SAMSUNG FOUNDRY

Power Management IP cluster: ready for migration to LN28FDS

- Total solution including support of Body Biasing

Power Management platform, SPEED PM: turnkey solution ready to support Power Management IPs once migrated to LN28FDS

WE TECH IT ON

DOLPHIN DESIGN

THE NEW BRAND OF

DOLPHIN INTEGRATION