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STRUCTURED DESIGN STRATEGIES

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Semiconductor designers are now in the business of system design and significant productivity improvements can only be reached through an additional investment upstream in architectural understanding. Chip layout strategies shall now result from such upstream decisions implying new developments in
- precharacterized cells used at the breadboard level,
- functional simulation using custom CAD tools.
Applications of parts of this thinking to a digital integrated circuit for a Telematics Controller of the 6805 family and to a Codec + Filter analog chip are presented.

I. ECONOMIES OF SCALE

Inadequate use of ratios and metrics across the Semiconductor Industry and related Research Centers is leading IC design engineers into inefficient design strategies. Some basic metrics must be reassessed.

Let us start on figure 1 with the most ordinary representations of the cost trade-offs of design and manufacturing between major design methods.
In view of these facts accentuated by the shortened design cycle-time of the easiest design methods, plus the general urge for custom design, it is but natural that a flurry of R & D projects have been started in favor of these easiest design methods.

A different representation on figure 2 enables us to look at another puzzling parameter which is too often forgotten in the debates : DESIGNABILITY. In other words "the easier the method, the more restricted its field of application". This "law" has been properly acknowledged by the VHSIC program [1] which takes as a measure of circuit complexity the product of the number of gates and of the IC frequency. Most handcrafted circuits involving analog components or dynamic logic could only be implemented with any "easier method" on some process technology of the following generation (e.g. : an analog modem can be handcrafted on a 1979 state-of-the-art process or can be designed with a symbolic technique on a 1982 state-of-the art process).

To complete the reassessment of traditional metrics, let us consider the regularity factor [2] on figure 3. The fact that an IC for an exciting 32-bit architecture can be designed with a much larger regularity factor than a more mondane 4-bit design, combined with the fixed cost inherent

to the chip input-output elements (I/O pads, buffers...) and the difficulty to make proper use of ROM or PLA techniques in them, all are biasing design productivity indicators in favor of the larger IC's. But such IC's also happen to have usually the smallest industrial impact (product volume). The risk inherent to this vogue is that wrong research problems are being emphasized and adequate tools are not being developped.

Note : there are scientific motivations for using the $ (or FF, etc.) as an optimization criterion. For instance, the only common measure between silicon area and test duration to assess the low-cost nature of a design is a "weighted average" expressed in $. Meanwhile a testable architecture can only be obtained at the expense of silicon surface.

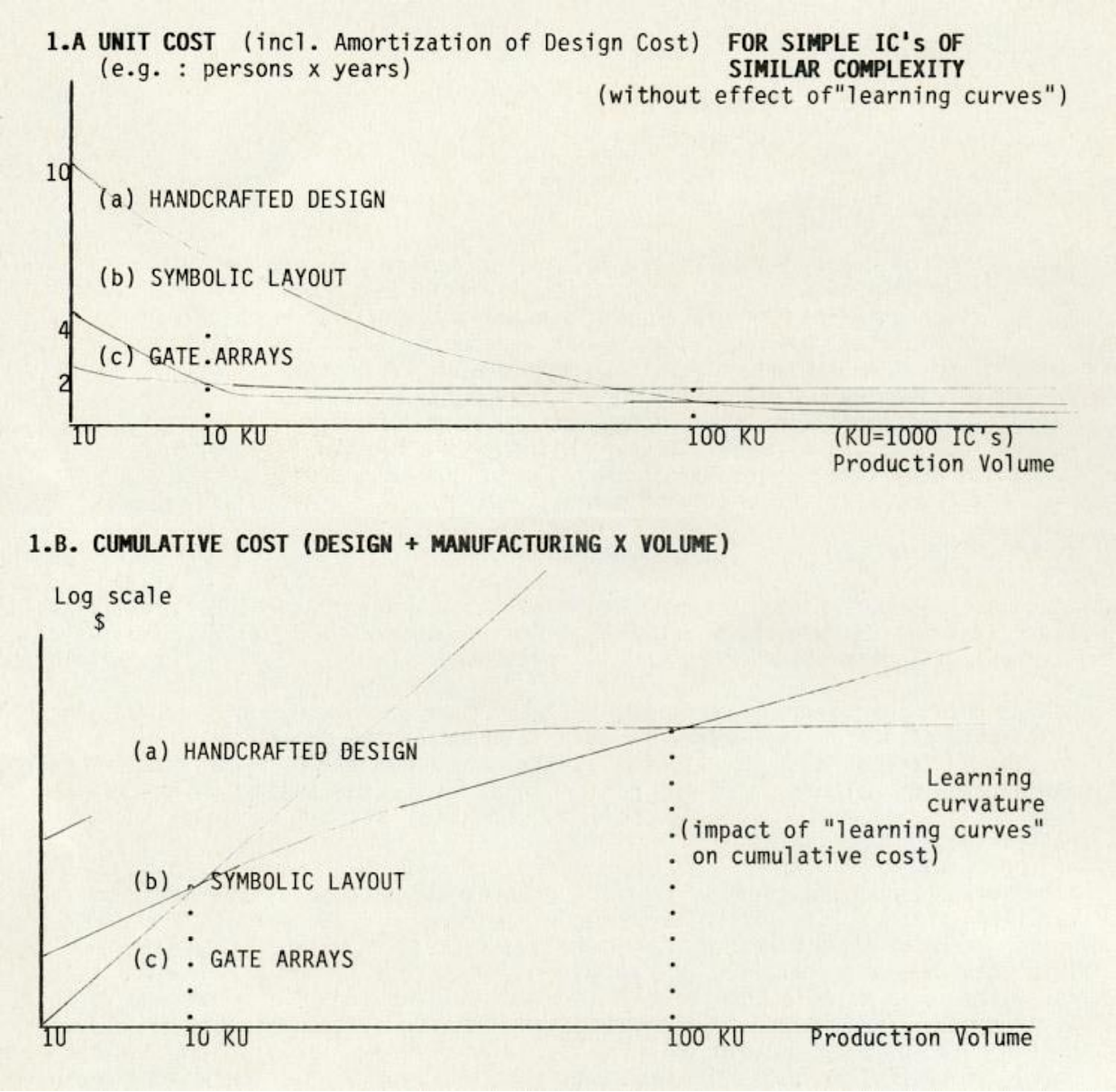


Figure 1.
Breakeven points for production quantities according to choice of design method.

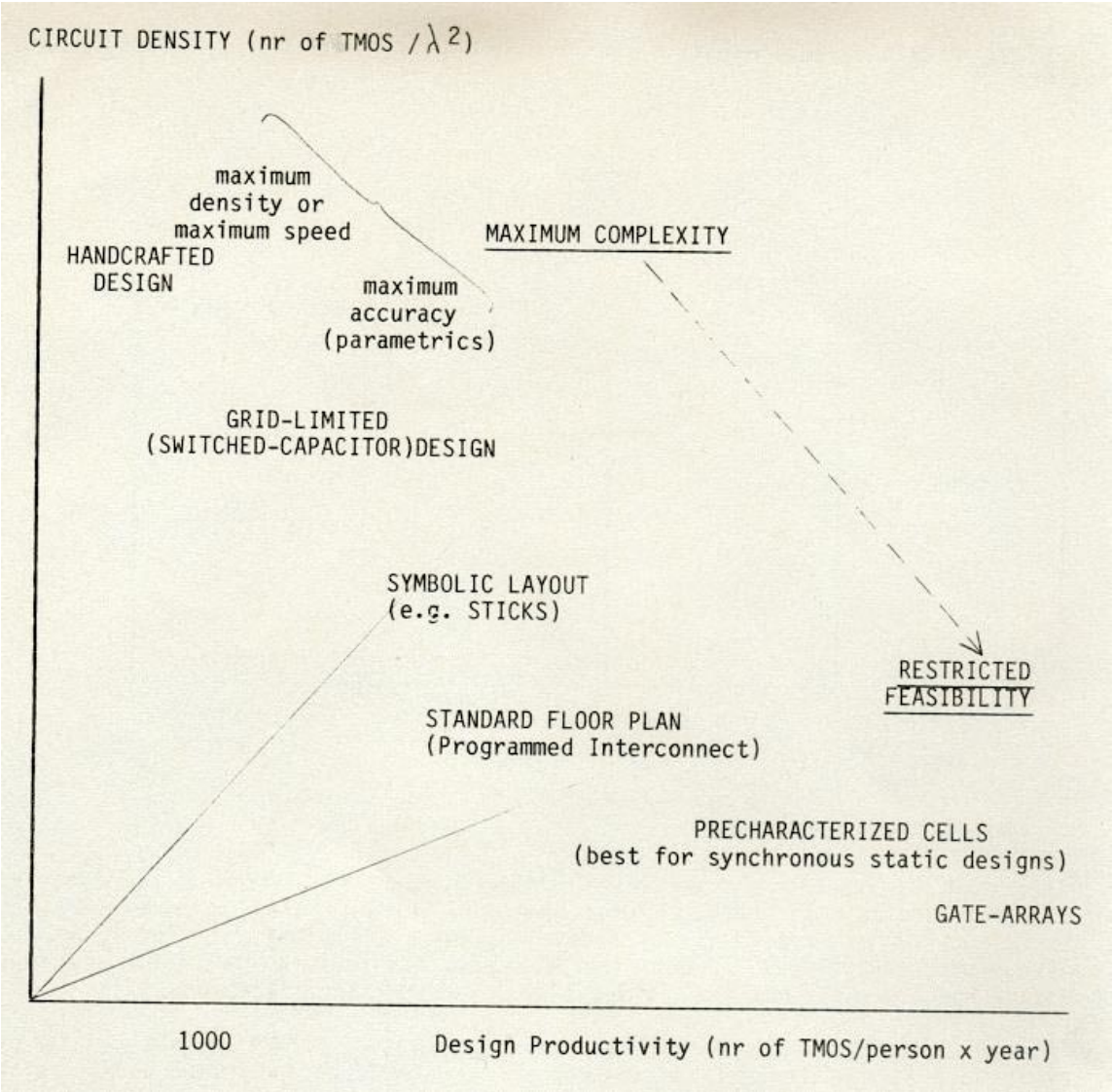


Figure 2.A. Trade-offs between Design and Manufacturing Costs
(for ICs of similar complexity).

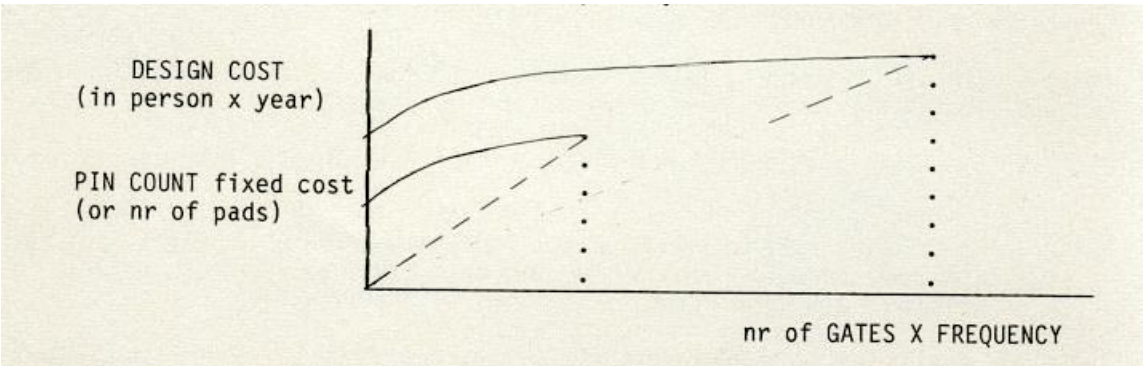
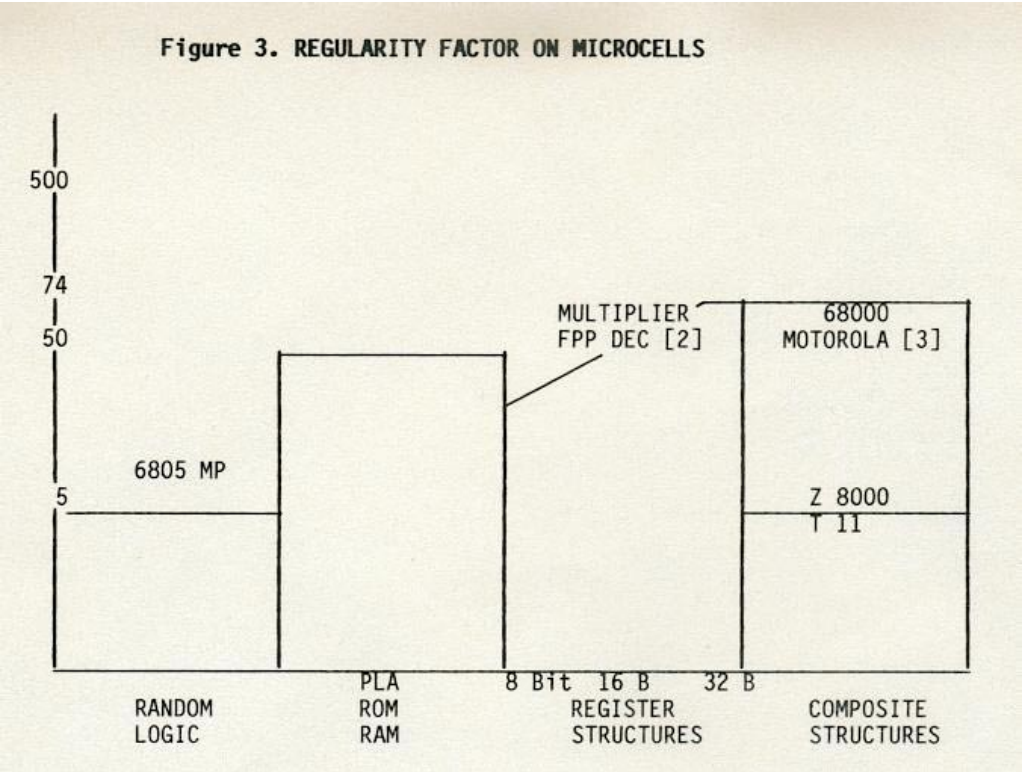


Figure 2.B. Design Costs (fixed plus variable) versus complexity
Statiscally showing higher productivity for larger circuits.



II. INTEGRATION OF SYSTEMNESS

I now want to present two intuitive notions not only there is a "learning curve" for design cost (notion of familiness of IC's), but it is best used when the designer also is a system architect. In such a situation the designer not only is more experienced and efficient but also can reuse parts of his previous designs whenever he identifies commonality in product specifications.

Figure 4 indicates why productivity measures related to the single metric of layout cost (transistor per person x year) are inadequate in VLSI : the major cost instead is associated with circuit structuring and prototype debug. The only acceptable productivity metric is the overall ratio "$/Transistor x frequency" if all design expenses related to the four major phases are accounted for, through Design Release to the Silicon foundry :

Phase 1. Circuit Structuring (establishment of benchmarks, functional simulation, testability analysis of architecture, self-test) [4].

Phase 2. Synthesis and layout (with logic simulation, circuit simulation, bread-boarding).

Phase 3. Prototyping (design verifications [5]: on Design rules, Electrical rules and Interconnects ; mask making and checking ; test pattern generation prototype production and process-control checking).

Phase 4. Design validation (prototype debug, application development, system correctness-checking, characterization, qualification).

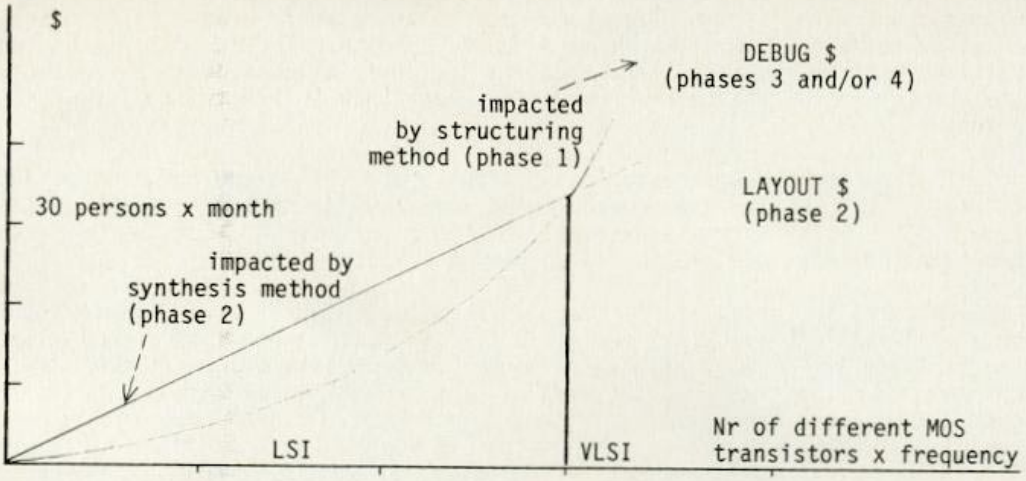


Figure 4. DESIGN COST : Layout was of prime importance in LSI ; with VLSI it is no longer.

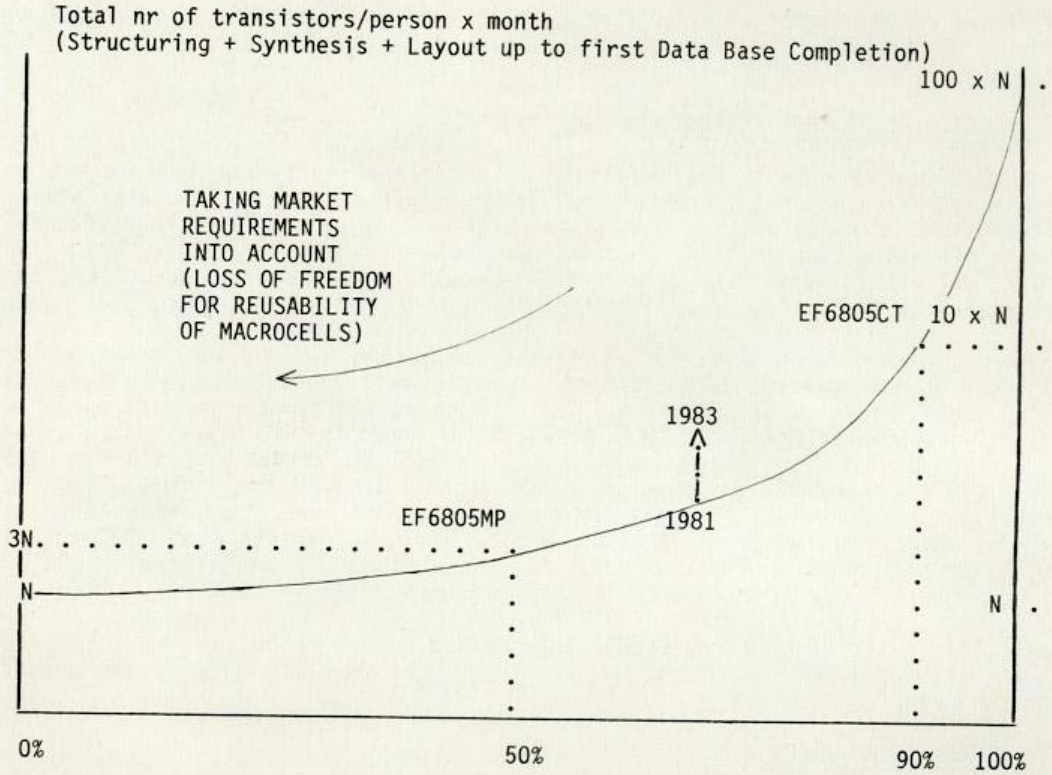


Figure 5. DESIGN PRODUCTIVITY / percent of reused macrocells.

As an example of the increasing cost of non-layout related expenses of a system level chip, a 1200 Baud modem IC can only roughly be verified in 15 minutes on equipments operating at the same clock rate as those which should perform the IC production test in 15 seconds. Phase 4 thus is crucial for identifying the physical laws specific to the IC and enabling the correlation of test parameters so as to safely shorten the test duration from more than 15 minutes to less than 15 seconds.

Also chip architecture and design methodology are basic to the duration of debug and test : for instance a microprogrammed structure is amenable to ROM testing followed by a self-testing sequence, a far more efficient debug or test technique than any technique applicable to random logic.

As a corollary, let us emphasize that, while an easy ride through Phase 3 results from a good job in Phase 2, an easy ride through Phase 4 requires a good job in Phase 1. Since the architectural job is at the system level, familiness of IC's makes possible the reuse of macrocells (e.g. a CPU, a multiplier, a filter, clocks and phase generators); the resulting impact is described on figure 5. Roughly speaking, if it takes 1 000 persons x months for a complete handcrafted VLSI design, 100 persons x months will suffice if 90 % of the IC is precharacterized and 10 persons x months will suffice if the macrocell kit is 100 % ready. Additionally the idea is not to solely reuse the layout data of previous circuit cells but also their schematics, their logical simulation and their test pattern.

Synthesis methods (repetitivity of microcells) can save percentages of productivity but structuring techniques (reusability of macrocells) can save orders of magnitude.

III DESIGNING BY ANTICIPATION

The major obstacle to taking advantage of microcell regularity is inherent to "software efficiency requirements" implying the introduction of innovative functional elements which destroy the repetitivity of topological features (e.g.dense coding of instruction fields). See our results on figure 5. Meanwhile, the major obstacle to taking advantage of macrocell reusability is obsolescence of process parameters or the need to design in the most cost-effective technology [6].

Pondering figure 6 leads us to the obvious statement : since we cannot design with the unknown process parameters of a technology 3 years hence, we must develop tools for Automatic Selective Sizing This is the first situation amenable to Artificial Intelligence (Pattern Recognition) where THOMSON-EFCIS has obtained rewarding results. The same microprocessor (EF6805 MP) compatible with the core of MOTOROLA 's MC6805P2 was produced simultaneously in NMOS (6µ channel length), HMOS-1 (4µ) and HMOS-2 (2µ) through automatic layout generation (only I/O pads require manual intervention). Whenever manufacturing economics switch the minimal cost from one technology to the next, the manufacturer is ready to make use of the next mask set without further designer's support.

Actually, in the case of the EF68O5CT presented below, the mere size of the IC in the technology of the initial layout would have been unacceptable for actual manufacturing.

IV HIERARCHICAL DESIGN

In order to benefit from macrocell construction techniques for VLSI IC's, the next urgent CAD development was a "Two-dimensional Word-Processor", i.e. a chip floor-plan editor which was developped by THOMSON-EFCIS and named CANVAS.

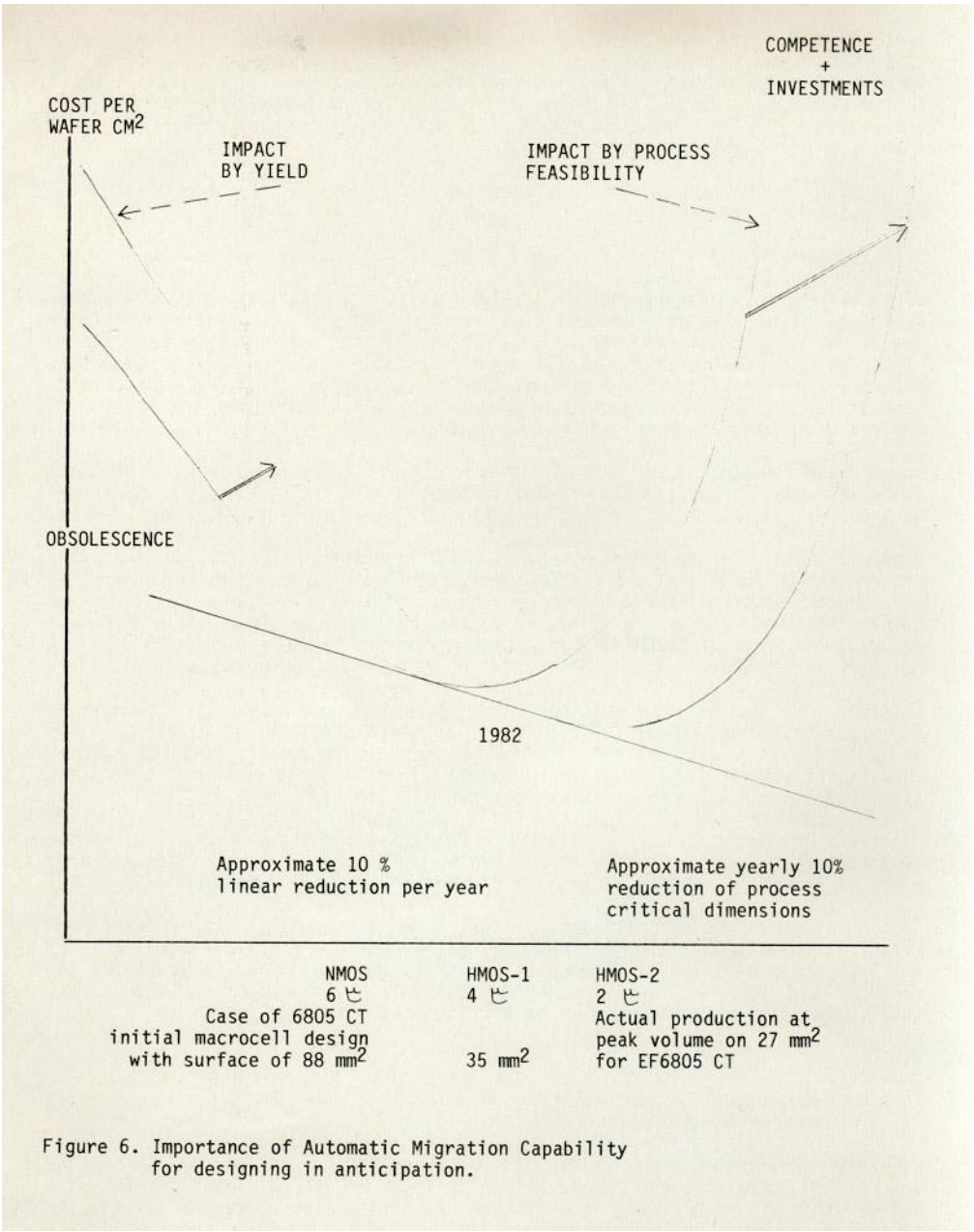


Figure 6. Importance of Automatic Migration Capability
for designing in anticipation.

The need to perform simultaneously the design tasks on independent subsets of a circuit (the macrocells) has introduced the need for new tools to check interfaces between the subsets. Previously existing CAD tools remain applicable within the subsets, while new CAD tools are required to manipulate the subsets as a whole (e.g. symetry, rotation, shrink) and to ensure proper cooperation both spatial and temporal.

The system-orientated designer now operates in either of two ways (and their combination) as follows.

A. Bottom-up

With the Benchmark requirements in one hand and the precharacterized cell library in the other, the designer edits his proposed chip canvas so as to minimize the amount of custom synthesis and layout work to be performed (5 % of custom layout may be considered as a good degree of "Non-Artificial Intelligence" to maintain a creative edge over pure macrocell reassembly). In other words, goodness of the design can be proven in sequential steps: first for the precharacterized macrocells, then for the custom cells.

In reference to phase 2, note that precharacterized cells can now be used for a quick assembly of the breadboard for customers ROM programming and debug, as well as for the design of an emulator for an Application Developpement System.

Figure 7 illustrates the real case of a 56000 transistor chip for the 8-bit microcomputer (EF68O5CT) with the EF68O5MP as its core. The core was extracted from the MC6805P2 acquired from MOTOROLA and engineered into a Telematic Controller by Edouard PRESSON's team. It was sampled to customers twelve months after agreement on design objectives (even though automatic routing between macrocells was not yet available). Compare to the State-of-the Art on 4-bit processors [7].

In order to illustrate the real complexity of this microcomputer let us mention its major cells besides the CPU : a RAM, a multiple size ROM, an elaborate timer and most of all a complex UART with independantly programmable Emission and Reception. It was totally simulated on the THOMSON-EFCIS logic simulator EPILOG and its first silicon was sampled to customers.

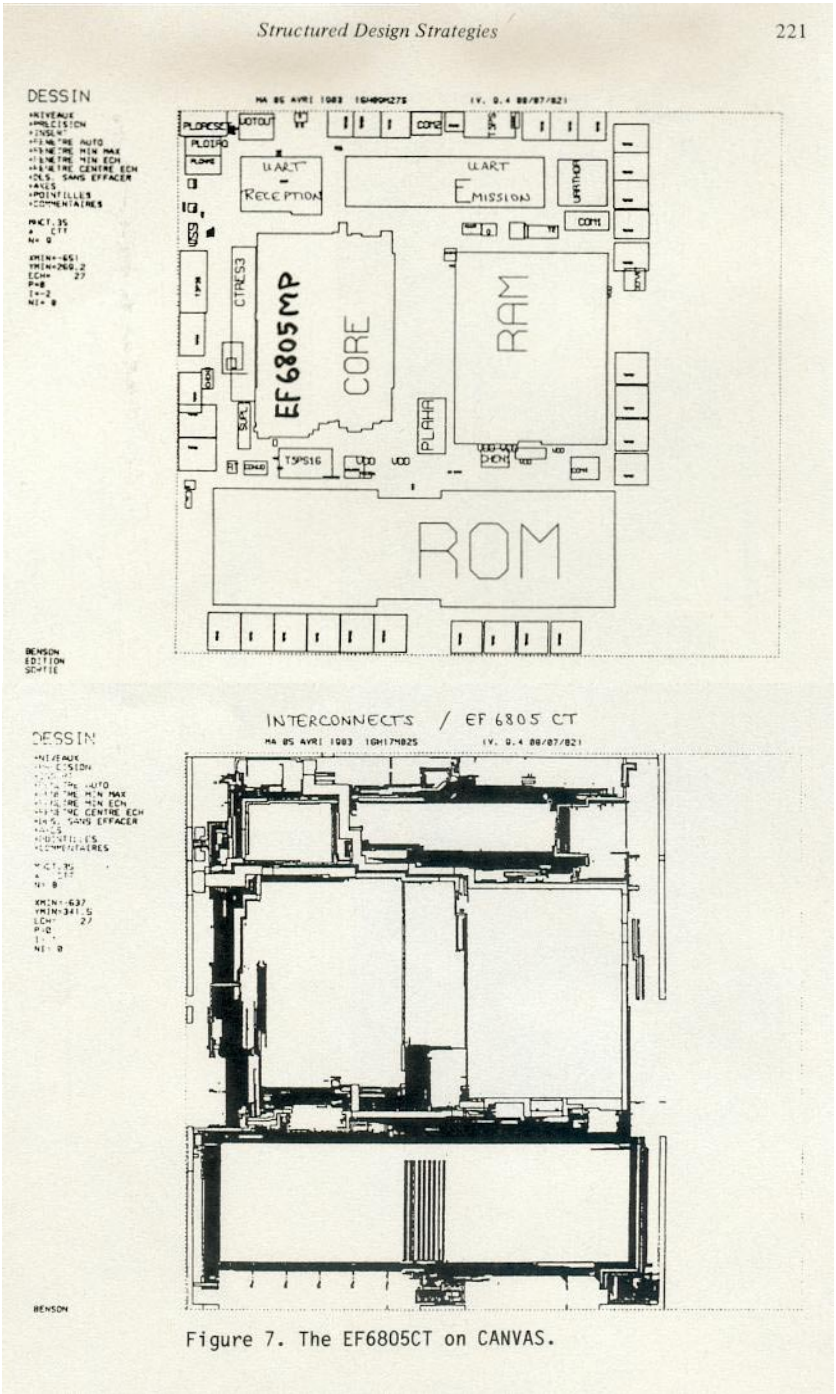
Finally migrating this design to the next technological process is a simple reassembly job, as long as the custom layout portions (10 %) have been prepared with the Automatic Selective Migration program presented in paragraph III.

Instead of aiming at a 16-bit design like the TI/AMI 9940 [8], it appeared preferable to select this 8-bit design for the CPU so as to offer simultaneously an HMOS and a CMOS set of macrocells. Up to the WAIT and STOP instructions the EF68O5MP and its CMOS counterpart the EF68HCO5MP are pin-to-pin compatible, which permits considerable savings in Development Tooling.

B. Top-down

This is supposed to be more abstract and therefore more classy : as a result, its drawbacks only are of interest to this audience.

Figure 8 represents a Codec+Filter PCM processor engineered at THOMSON-EFCIS by Jean Claude BERTAIL's team for telephone applications. It was designed in twice the duration of the previous chip with the most effective degree of parallelism (4 layout persons). 40 % of its surface is digital (3200 transistors), the rest is analog (switched capacitors and 1500 transistors). The digital portion was fully simulated on a digital simulator, while the difficult zones only of the analog portion were simulated on the electric simulator SPICE from BERKELEY.



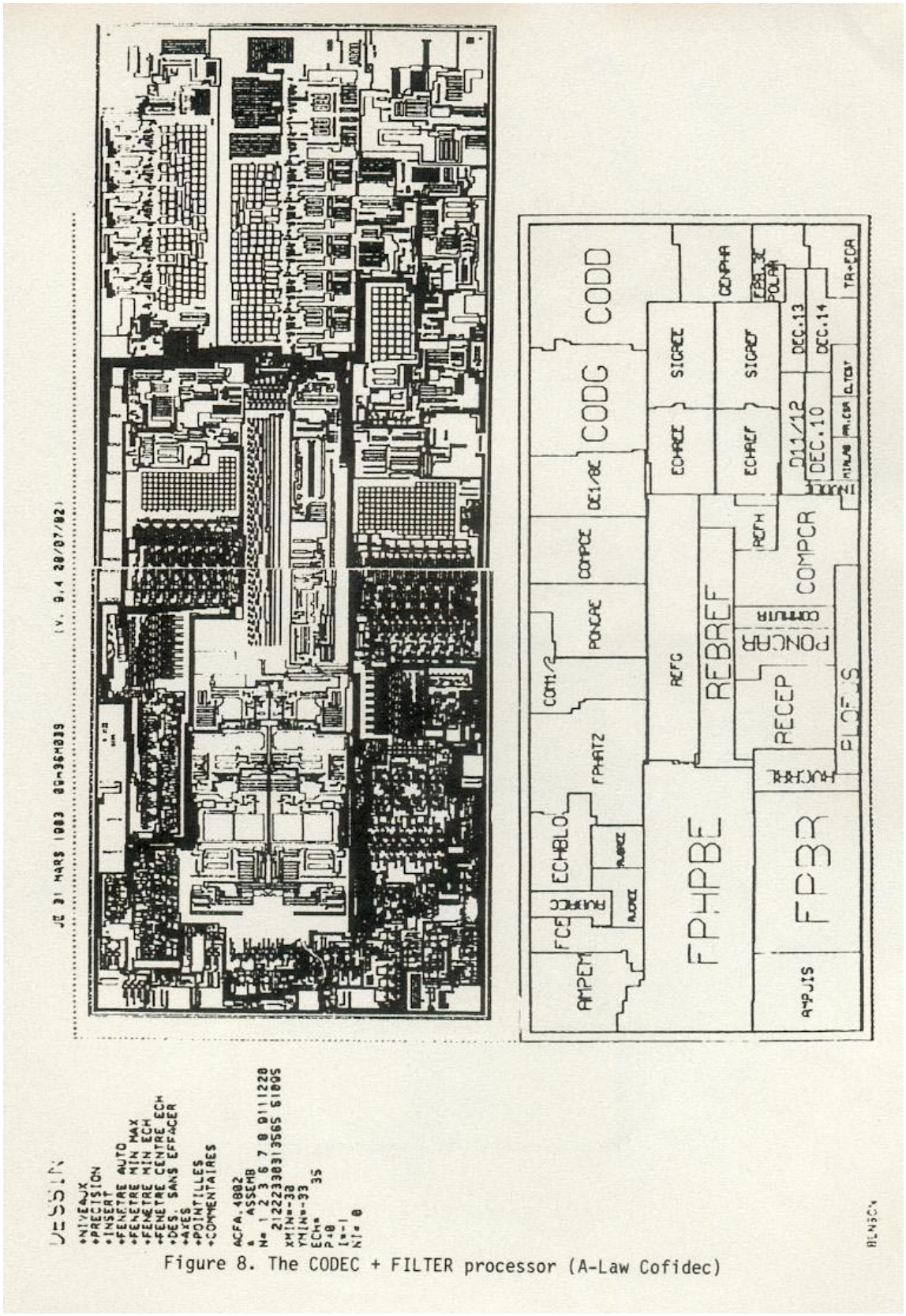


Figure 8. The CODEC + FILTER processor (A-Law Cofidec)

- The primary drawback is that all macrocelis have to be designed at the same time. They not only compete for attention but they are all based on equally unproven assumptions of goodness leaving too many degrees of Freedom and the phenomenon of "uniform suspicion". The general consequence is that difficult macrocells will get the best attention and the easy cells will come out with defects ! Another consequence is the absence of a firm specification of macrocell interfaces leading to design errors on the interfaces.

- The secondary drawback results from the difficulty of area budgeting for new macrocells so that blanks will appear between densely handcrafted cells (at best as the result of overbudgeting in one cell, at worst as the result of underbudgeting in one cell which results in the need to fix through the spliing of several nearby cells on the same line or column within the IC).

V. CUSTOMIZATION

Structured hierarchical design methods should be advocated for the largest number of small design teams with the following words of caution

A. They should not undertake large topdown designs but should concentrate on bottom-up designs with precharacterized cells.

B. All design teams should focus on obtaining guarantee of automatic technological migrations by the silicon-foundry.

C. Small design teams should not take the risk of dynamic, asynchronous and fast circuit synthesis which push the technology to its ultimate performance (requirements for parametric accuracy, etc.).

The latter kind of designs should be reserved to highly specialized professionals making use of topdown handcrafting techniques with the close support of a manufacturing team.

D. Silicon-foundries should place their energy on offering the largest menu of customization tools metal-level variations on a set canvas; metal-level programming of ROM's or PLAs; use of EPROM's

VI. SOME REQUESTED R & D EFFORTS

The present emphasis on structured digital design has lead to neglecting the problems related to mixed ICS integrating both linear and digital cells. For instance see Figure 8 for the A-Law Cofidec (Si-gate CMOS).

A. While series 74TTL-LS and 74HCMOS have lead to a STANDARDIZATION of elementary precharacterized cells, there is no such status for the analog portion (switched capacitors, operational amplifiers, etc.).

For the above-mentioned Cofidec a topologically equivalent breadboard was constructed : while 30 % of the IC is digital and 70 % analog, the breadboard was made of 5 large analog boards

(double Eurocards) and only one digital.

For a similar reason, the large majority of gate-arrays are merely digital.

B. Microcomputers are now limited in capability for the unability to integrate analog peripherals. Industrial Testers have been specialized either digital or analog and a circuit combining macrocells of both kinds is at best difficult to test with effectiveness. Moreover testability studies have been focused on digital designs and little is known for the analog cells (what is a testable filter design ?). Analog peripherals within microcomputers can now benefit from the autotest capability of the microprocessor core to relieve the industrial tester of the expensive task of analog testing. This is a reenactment of the INVERSE POWER Principle well-known for computer testers in the early 70's.

C. For the sake of ultimate "Interconnect Verify", it is necessary to make use of digitized schematics, homogeneous across the analog/digital boundaries and usable directly as the IC description for a pin-to-pin simulator. But there is no such simulator today available (logic/analog, pin-to-pin, with effective modeling capabilities).

It should also be complemented with a postprocessor for transferring correct test-patterns to such industrial testers mixing digital and analog.

E The difficulty with mixed industrial testers is partly due to the absence of a simplified I/O representation for analog signals in the time domain. While this is true also for electrical simulators (SPICE-like), such simulators suffer from a congenital deficiency : they require a modeling job supplementary to the design task. In effect, it is not sufficient to demonstrate the electrical simulation is correct. Instead it is necessary to prove that the simulation model is equivalent to the graphical representation of the IC (layout artwork). The only solution resides in a 'chip model extractor" or equivalently in a SPICE-like simulator which would accept the layout as IC description (much like "Design Rule Checks" operate on the layout data base, or logical simulators on the digitized schematics).

E. Assembling macrocells for large circuits is one thing, but not wasting various parametric budgets (surface, timing, accuracy, power consumption, offset, frequency ...) on a truly complex chip is another challenge. Tools for distributing the parametric budgets to the macrocells cooperating in the chip are required.

F. Overemphasis on the area minimization issue is masking the true goal of yield improvement. Much remains to be done in design sturdiness : reduction of the number of mask layers and reduction of sensitivity to design parameters (cutoff frequencies, temperature ...). Surface is no longer the primary factor to good yield.

But better evaluators of such varied requirements, other than merely the transistor count, can only result from a more thorough understanding of system function complexity (not amenable to Artificial Intelligence).

A CALL FOR SIMPLICITY

Hierarchical design must not be confused with a proliferation of inconsistent design representations. It rather means a progressive focusing of the design representation, starting from the objective specification up to the artwork and test files, through the smallest possible number of intermediate models.

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