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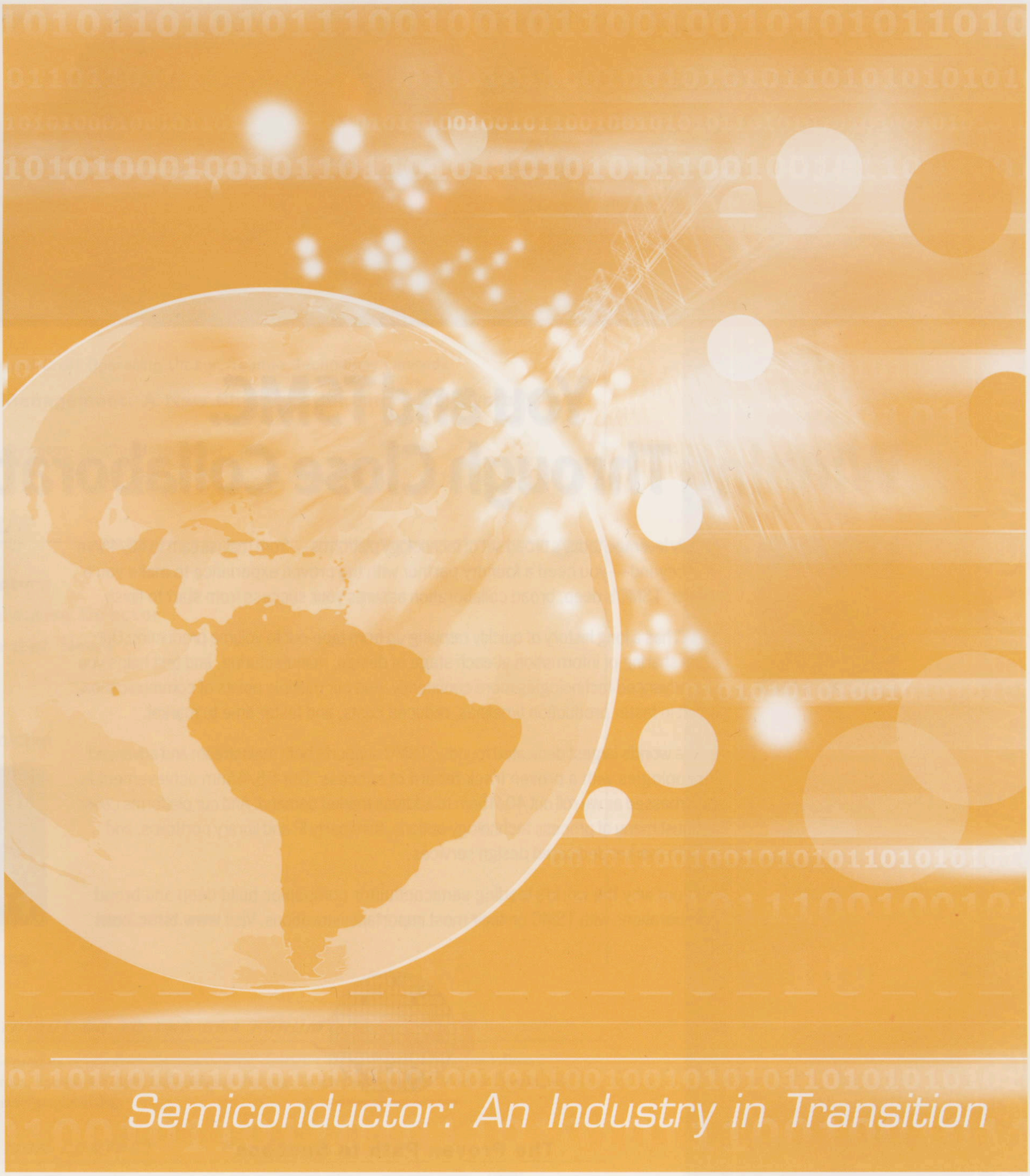

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Embedding Power Management: A New Challenge for Improving System Competitiveness

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There is an increasing frenzy to integrate multiple digital and analog functions in mixed-signal systems-on-chip (SOCs). Integrating power management is part of this trend, but raises new issues for SOC integrators; selecting ICs for power management was traditionally the domain of printed circuit board (PCB) designers who could benefit from off-the-shelf products aplenty.

This trend is now fuelled by the availability of new silicon intellectual property (IP) for power management – virtual components (ViCs). Therefore, embedding such functions now becomes the responsibility of SOC integrators who must face the corresponding challenges: (1) identifying the relevant specifications for such embeddable voltage regulators and (2) having a knowledge of the intrinsic noise, how to specify the capability of filtering Global System for Mobile Communications (GSM) burst noise, the transient response, the capability to drive analog or logic loads and which models should be used for simulation at the SOC level.

What is at Stake: Benefits and Challenges

To justify embedding power management solutions, SOC developers must consider the advantages for their own products, as well as for their users' electronic systems. There are mainly three benefits from embedding power management functions within a SOC:

- Reduces the physical volume of electronic systems.
- Reduces the bill of materials (BOM).
- Increases performance and reliability.

Embedding power management achieves these goals by:

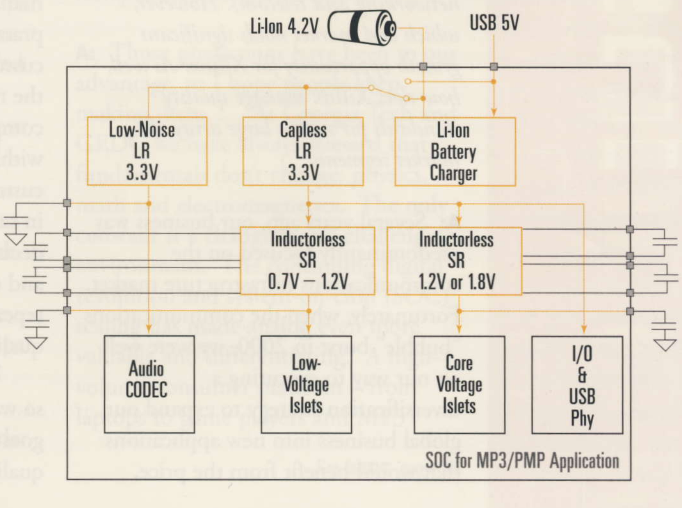
- Reducing the number of voltage rails required to supply the SOC.
- Supplying SOCs directly on a standard battery such as Li-ion, Li-poly and alkaline.
- Regulating supply voltage internally and eliminating PCB and package parasitic effects, which deteriorate the quality of voltage supplies required for high-resolution applications such as audio and radio frequency (RF) circuits.
- Enabling design with voltage islets, thus allowing voltage scaling and dynamic power consumption control of the SOC.
- Reducing the complexity of board-level design, the number of external passive components and the overall system BOM.
- Increasing the level of integration of the whole system.
- Reducing the dependency on several providers of ICs and passive parts.

Consequently, embedding power management solutions is more than a "make it smaller" game. It improves SOC product competitiveness by enabling better regulation performance, flexible power consumption control and lower production cost for the whole system.

A Typical Application Taking Advantage of an Embedded Power Management Solution

As an example of the advantages previously listed, Figure 1 shows a power management solution for a MP3 player SOC. This integrated power management solution includes a battery charger for a Li-ion battery, a 5V-tolerant "capless" linear regulator (LR) providing an internal 3.3V digital supply, two inductorless switching regulators (SRs) supplying the SOC digital core and memory, and a 5V-tolerant, low-noise LR supplying the sensitive audio circuitry of the

Figure 1. Integrated Power Management Solution for a MP3 SOC



SOC. This SOC now works on a single supply provided by the battery, making the life of board-level engineers much simpler. The supply of the sensitive audio circuitry is internally regulated by the low-noise LR, ensuring minimum supply noise and optimal audio performance. A capless LR is key to any embedded power management solution, as it enables internal regulation without requiring any additional pin or external component. The integrated inductorless SR exploiting two cheap ceramic flying capacitors eliminates the costly and bulky inductor and maintains good power efficiency. It allows for internal voltage scaling, enabling dynamic power consumption management in different modes of SOC operation. With such an integrated power management solution, the SOC is self-sufficient, with regard to its own supply requirement.

Facing SOC Integration Challenges

Integrating power management ViCs still raises concerns in the SOC integrator community because success or failure of such integration relies on a ViC's behavior in the SOC environment. The "ideal embedded voltage regulator" must provide:

- A cost-effective solution that occupies a small silicon area and requires few external components or none at all.
- A safe and predictable integration, taking into account all possible and undesired couplings with the rest of the SOC.
- The best tradeoff between regulation performance and power efficiency over all operating modes.

ViC providers must deliver the appropriate specifications, provide the means to check that such specifications meet specific SOC requirements and highlight possible hidden integration effects or traps. In addition to the usual voltage regulator characteristics, such as input voltage range, output voltage range, efficiency and maximum load current, important application criteria must be taken into account to specify the appropriate LR or SR for safe embedding into the SOC.

Current Consumption Profile of the Circuit to be Supplied

There is no single figure able to qualify the current consumption profile of a circuit to be supplied. The average current consumption is definitely an important data input, but over time, the current demand may vary significantly depending on the circuit type (digital or analog) and circuit activity (standby mode, low-power mode, etc.). What is at stake includes:

- The appropriate output stage sizing to guarantee the voltage regulator has the driving capability to support the current required by the circuit to be supplied.
- The necessity to have or not have a capacitor on the regulator output, and to properly evaluate its value.
- The silicon area of the ViC itself, which is quite sensitive to the driven load.

What is required includes an appropriate electronic design automation (EDA) solution and associated models to:

- Estimate the current consumption profile of the circuit over time, based on simulation in the various operating modes.
- Extract the relevant parameters required to properly size the output stage of the regulator.
- Check that the parameters associated with a specified regulator are in accordance with the current profile of the SOC or a subpart of it.

Such solutions exist today, and power management ViC providers must make them available to their users to eliminate any integration risk.

Bill of Materials

Reducing the BOM goes along with reducing the number and the cost of external passive components required by the power management ViC. Indeed, some ViC providers now offer competitive alternatives for both LRs and SRs.

Two types of LRs are offered to SOC integrators: regulators with an external output capacitor and regulators without an output capacitor. In an integration context, it becomes obvious that capless solutions are more attractive because they reduce the number of pins and external components, especially for complex SOCs built on several voltage islets. However, since capless regulators do not have an energy tank on their output to deal with sudden transient current surges, cautious validation using dynamic current consumption of the SOC must be conducted, as previously mentioned.

On the SR side, inductor-based regulators have historically represented the preferred architecture for power supplies. Now, in low-power and integration contexts, inductor-based SRs show several limitations that can be overcome by the use of inductorless SRs.

The first and foremost important limitations of inductor-based SRs are the cost and the size of the inductors. In most cases, inductors dominate the cost and the size of the integrated SR solution. To address this, consumer product engineers dealing with cost constraints are tempted to choose cheaper inductors that dissipate more power and significantly reduce SR power efficiency. Consequently, good power efficiency, the main advantage of inductor-based SRs, vanishes. On the other hand, inductorless SRs exploit only one or two small, cheap ceramic capacitors instead of an inductor. Those SRs, also called "charge pump converters," have been known to be less efficient than their inductor-based counterparts when used with a variable input voltage. However, this is no longer true since multimode inductorless SR products are now available and can provide an average efficiency over a typical battery voltage range similar to inductor-based SRs. Inductorless SRs are then a cost-effective alternative to consider when selecting integrated SRs.

Noise Sensitivity of the Circuit to be Supplied

An important application criterion is the noise that can be accepted on the SOC circuitry supply. The noise on the voltage supply provided by a regulator has two contributors: the intrinsic noise generated by the regulator itself and the noise coupled from the regulator input to its output. Regulator specifications must include a complete power supply rejection ratio (PSRR) and graphs of intrinsic noise versus frequency. The SOC integrator's task is then to compare these graphs with a "power noise tolerance template" of the circuit to be supplied. This can be quite critical for circuitry sensitive

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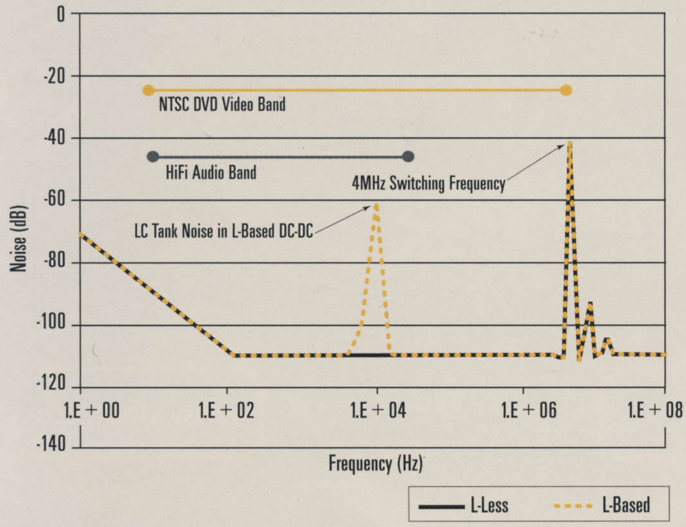
to noise such as audio or RF. Figure 2 illustrates the intrinsic noise (deterministic, including ripple and random, including thermal); for an inductor-based SR, the noise is distributed around the inductor-capacitor (LC) tank resonance frequency formed by the inductor and the output capacitor. This frequency may often be within the audio or video frequency range, making the direct supply of audio or video converters on the SR output risky. Inductorless SRs have a fairly flat intrinsic noise profile. Typical intrinsic noise profiles are illustrated in Figure 2 for both SR types.

Figure 2. Output Noise Profile for an L-Based and L-Less Switching Regulator



Power Efficiency, More Than a Single Number

Efficiency is usually not well understood by users since it is expressed as a single number, which is meaningless and could even lead to a wrong decision. What is important is not the peak and somewhat hypothetical power efficiency, but the average efficiency (considering the variation of the input voltage) over the battery's lifetime for instance. Integrators must be aware that maximizing SR peak efficiency, which is often specified by IP vendors, does not necessarily minimize the average current consumption of the SOC. In all SR solutions, efficiency varies with input voltage and output current. Therefore, when maximizing efficiency, SOC integrators must take into account the battery voltage variations on which the system works and the SOC current consumption variations in the different operation modes of the SOC. To do that, IP Vendors should always specify the efficiency of their solution as a function of input voltage and output current.

In addition, SOC integrators must never forget that when the difference between the regulator input and output (dropout) is less than 10% of the output voltage, LRs, also called low dropout (LDO) regulators, are as efficient as SRs. For example, generating a 3.3V supply from a Li-ion battery providing a 3.6V average voltage for most of the discharge time is done as efficiently by a LR, but with much less silicon area and external components.

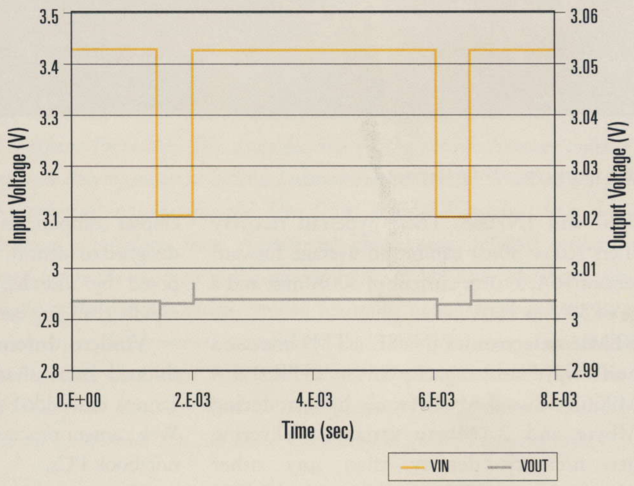
Compatibility with High-Voltage Sources

Another application issue common to portable systems is a supply voltage over 3.6V (e.g., a 4.2V Li-ion battery and a 5V Universal Serial Bus (USB) power line). Since generic CMOS processes do not tolerate more than 3.6V, specific design techniques must be used to prevent regulator transistors from being exposed to voltages higher than 3.6V, even in shutdown conditions. Therefore, ViC providers must specify in their documentation that such techniques have been used to guarantee long-term reliability of the regulator.

Protection against Violent Supply Perturbation

A voltage regulator's capacity to maintain their output voltage at the desired regulated value may be critical in specific applications, such as mobile phones, where violent changes in input voltage are experienced. This is called the transient response characteristic. To ensure the integrated regulator can deal with such transience, the expected amplitude and duration of this behavior must be identified and the regulator validated in simulation under these conditions. As a typical example, the Time Division Multiple Access (TDMA) burst, applying up to 1A on the battery of a mobile device at the 217Hz rate, may create a drop higher than 300mV on the battery voltage. LRs must be able to absorb this voltage drop without changing their output voltage, especially if they supply sensitive analog circuits such as an audio amplifier. Otherwise, audio quality may be altered each time these TDMA bursts occur. Figure 3 depicts the capacity of a LR to reject such bursts, maintaining a very stable and quiet 3V voltage at its output.

Figure 3. TDMA Burst Rejection on a LR



Conclusion

Embedded power management in SOCs is now practicable, but specifying the appropriate regulator as a product demands close cooperation between the SOC integrators and the ViC provider. The ViC provider must understand the application constraints and properly specify and package the ViC so SOC integrators can concentrate on their own tasks, allowing a safe integration. ■

About the Author

Yves Gagnon is the manager of Dolphin Integration's subsidiary in Montreal, Canada and is in charge of the development of power management ViCs. Yves had previously founded and been chief technical officer of LTRIM, a company specialized in power management solutions. You can reach Yves Gagnon at di-inc@dolphin-integration.com.