IP/SOC 2005

Session: Industrial Design and Methodology

IDRT-aware SoC Integration Flow

by Andréa Bonzo, Lucille Engels, Frédéric Poullet
Dolphin Integration
Meylan France

Abstract
Systems-on-Chip integrators are facing the need to integrate the mixed signal virtual components, which best perform sensitive I/O functions. They must address hierarchically the interactions, instead of the traditional approach operating flatly on the lowest level, as this suffers from a double-whammy, as follows.
A new integration process must make room for the innovative concepts of subdivision into power-supply islet but also for the quantification of the "Injected Disturbance Rejection Threshold" (IDRT) of noise sensitive virtual components.
We thus present a novel approach to mixed signal SoC Integration, namely a hierarchical IDRT-aware SoC design flow.
The dual key points in such a design flow are on the one hand floor-planning with islet definitions for level-shifting and macrocell placement, and on the other hand assessments of resilience to disturbances in view of disturbance sources in the Rest-of-SoC. Ultimately, Virtual Sockets as promoted by VSIA enable hierarchical verifications through simplified representations of hard components at appropriate levels: DRC, LVS, ERC, STA, and more…

IDRT-aware SoC Integration

As SoC optimization becomes more and more complex, in a multi-dimensional constraint space, it is no longer acceptable to perform optimization under a single constraint, either area or speed, but now power consumption and disturbance control must also be taken into account.
The traditional flat approach using a single bulky Place and Route solution with a single optimization criterion is no longer satisfactory, as it is necessary to allocate budgets for parallel developments of the several subsets of Virtual Components (ViCs).
Modernizing drastically the SoC design flow is required, thus switching to a truly hierarchical approach with ground plane placement, hierarchical verifications with blinded levels, and islet power-supply subdivisions, in due respect of Injected Disturbance Rejection Threshold (IDRT).
In other words, not only managing the interactions between diverse and complex components requires an upheaval of methods, but also the quandary of preserving the resolution of high precision analog is added on top.

To a new 4-rail standard for a cell library
The power consumptions, both dynamic and static, become more and more critical for portable applications, which tend to be mixed analog and digital. The constraints in term of power consumption depend on the final application:
- for Wi-Fi, the target is a battery life of one day and both dynamic and static power consumptions have to be minimized
- for Bluetooth, the target is one week: static consumption becomes prevalent
- for ZigBee, the target is a battery life of one year: static consumption is definitively is the sole criterion to be minimized.

Moreover, with the drastically increasing number of functions embedded in a SoC, transistor leakage overwhelms the "very deep-submicron" circuits.
To solve the quandary of more functions for longer battery life, without waiting for the completion of place and route to acknowledge its failure, a solution is proposed at post-synthesis level (firm) based on IDRT Characterization and Emulation processes, and on a library of standard cells with mixable optimization rules.

Library basis for IDRT-compliance
One common design target aims at synthesizing with some constraint of minimum speed while minimizing power consumption. Consider alternately a SoC having as primary objective to reach some threshold of low dynamic power consumption, say with a stringent figure of maximum dissipation, with the complementary goal to maximize performance in processing speed.
Typically, the cell library (SESAME) has been assembled with a new standard so that its complete High Speed option serves to generate the first-pass gate level netlist.
After a power analysis and a localisation of "hot regions", a second stage consists in substituting cells from SESAME Low Power option to reach the power budget of maximum dynamic dissipation.
This structured synthesis process associated with a couple of SESAME options enables to attain methodically any such composite set of a constrained optimization objectives for design.

Deep-submicron technologies require a new look at the cell library standards. Their paradigmatic change is about leakage currents. A new 4-rail standard, enabling to switch alternative power lines, improves the performances of a SoC by decreasing drastically the leakage of the logic blocs through voltage scaling at the standard cell level.

Emulation for IDRT-compliance

It is remarkable that the early emphasis on the importance of testchips for silicon qualification of a ViC has been oblivious of the crucial importance of the nature of its Testbench. In the absence of a StressInside™ emulator on the testchip, no measurement on an analog component can be useful as its performance might be destroyed by the disturbances from the rest-of-SoC.

The Dolphin solution to this conundrum is based on a set of Virtual and Software Components forming consistent suites for the SoC Integrator (TIDE™) for the IDM (CHIDE™) and for the user of the SESAME library options (CHIMES™).

Islet Introduction

To handle the challenge of embedding millions of transistors for analog and digital components, it is mandatory to switch from a flat design flow to a truly hierarchical design process further subdividing into homogeneous power-supply islets. An islet is a part of SoC which is structurally independent, in term of power supply rails, from the rest of SoC. The hierarchical floor-plan activity starts with the placement of macrocells, the definition of islets and the insertion of level shifters to go from one islet to another one. Each macrocell is designed and optimized as an independent block, much as any ViC, with the sole difference that we refer to a ViC when the provider is a separate entity while the SoC Integrator designs his own Macrocell.

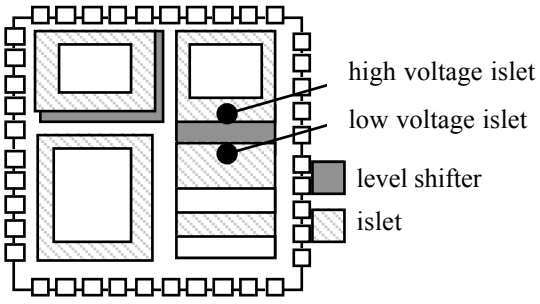

Figure 1: Islets repartition at SoC level

IDRT-aware placement

The "Injected Disturbance Rejection Threshold" serves to identify the virtual components which are noise sensitive and the noise sources and then to drive the hierarchical floor-plan, NECESSARILY FOR FINAL ACCEPTANCE OF THE FLOORPLAN PRIOR TO TOP-LEVEL ROUTING. The wise SoC Integrator has no use for an "extraction-based" analysis of disturbances after the expense and travails of Place and Route. In a mixed-signal SoC, the global disturbances generated may destroy the performances of analog ViCs embedded for reasons of SNR, THD, or jitter. The first stage in the IDRT methodology is the evaluation with CHIDE™ of the disturbance rejection ability of noise sensitive ViCs through the use of "Disturbance Rejection and Impact" (DRI) models for each analog ViC, unless duly supplied by the IP Provider. In any case the evaluation is mandatory with TIDE™ of the noise source macros through the use of "Disturbance Generation and Propagation" (DGP) models for the Rest-of-SoC through simulations at top level. Ultimately, the hierarchical SoC floor-planning is noise-driven: macrocell placement must take into account the simulation results, the disturbance source assessments, and the noise budget allocated. If the noise budget is overrun, the SoC integrator shall perform a power-supply tree optimisation with decomposition into skewed islets.

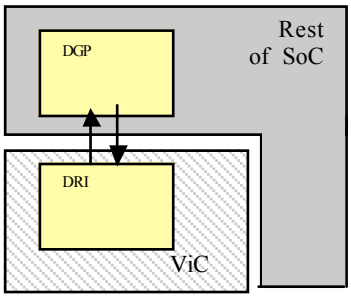

Figure 2: IDRT evaluation at SoC level

A hierarchical approach

The importance of developing Macrocells with the same rigor as ViC could not be overstated! The discipline and the advantages are clear when they all can be placed on Virtual Sockets. The hierarchical SoC integration process then is top-down. Indeed once the SoC integrator has fixed the floor-plan, the hierarchical characteristics are determined or budgeted. The Sockets are then fixed for the rest of the physical implementation. Following this, the new stage consists in handling the multiple power grid placements for powering-up the different islets. Each macro, represented by a Virtual Socket, has a separate implementation with clock tree insertion, standard cell placement and timing driven routing. The hierarchical routing is performed at top level with clock tree and buffer insertion.

An ultimate set of verifications

VSIA sockets provide the irreplaceable solution to perform hierarchical verifications at various levels through appropriate representations of macrocells. Each representation provides a simplified description of the macrocell for a set of hierarchical verifications, with identified speed accuracy tradeoffs, allowing detection of errors at earlier

steps in the design chains. Such representations may be comprised of one or more associated views and/or data files, which is why a separate EDA application, such as SoC GDS™, is needed for implementing them with specific care for: DRC constraints, LVS constraints, ERC, timing, leakage and dynamic power figures, as well as IDRT for noise injection and resilience.

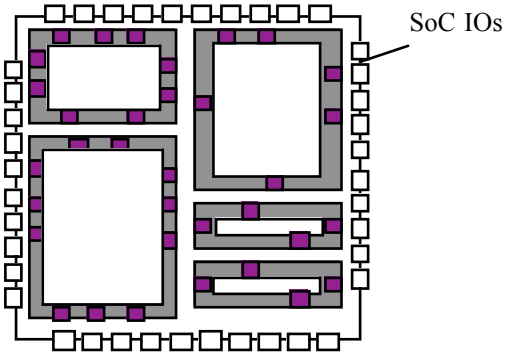

Figure3: SoC as interconnected sockets

Such extended Virtual Sockets enable the SoC Integrator to start the overall verifications just after macrocell placement, at the beginning of the physical implementation so as to detect the integration problems at an early enough stage to fix floor-planning and Disturbance propagation chokes. As the sockets are defined after the hierarchical floor-plan stage and can be used for multi-level hierarchical verifications all along the different stages of physical implementation, the DRI and DGP models, developed for simulation purpose, enable to define the IDRT sockets at the right stage of SoC Integration.

Inclusion of islets in Virtual Components

As a Virtual socket must be considered as a Black Box, it must be assumed that an islet may be predefined within a ViC with clear boundaries on the socket. In case the SoC could be defined totally as an assembly of ViCs, purely surrounded with routing, it appears that level-shifters might be needed for proper interconnections, unless they have been properly foreseen at the time of top-down budgeting and ViC specification. Duly avoiding contiguous level shifters inversion and transparent voltage transitions, contiguous islets within nearby ViCs thus partake in an overall on-SoC islet.

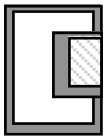

Figure 4a: Socket with clear boundaries

Virtual Component

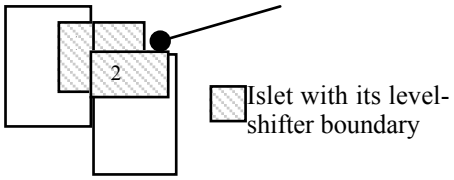

Figure 4b: Contiguous islets in different ViCs

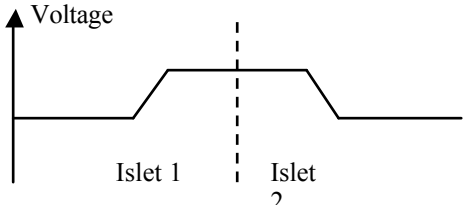

Figure 4c: Cancellation of inverse shifters on contiguous islets

Many simple intertwined concepts

While VSIA has invited us for years to proceed with a hierarchically structured design process, the practice has remained as undisciplined as before, and no sufficient EDA Solutions were offered for simple tasks as the formatting of Virtual Sockets. Even most definitions were lacking: by proceeding step by step, an innovative approach has emerged which convinces that the integration of a high-resolution mixed signal SoC no longer is black magic.