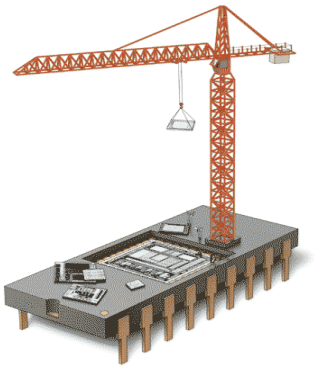
Cooperative Design-In Process from SIP to SoC



Jean-François POLLET - Product Line manager
DOLPHIN INTEGRATION - Meylan - France
www.dolphin.fr

IP99 - 22-23-24 March- Santa Clara

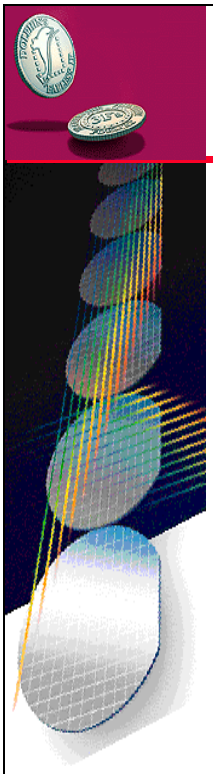
-**Change of era from ASIC design to SoC integration**

For more than two years, the Virtual Socket Interface Alliance (VSIA) has put lots of efforts and enthusiasm towards establishing technical specifications and facilitating the use of Virtual Components in the System-on-Chip (SoC) design-in process.

But technical specifications are only one part of the concern which a VC Provider has to address with the SoC Integrator. The efficiency of integrating a VC into a SoC has to face a lot of hurdles: legal, commercial, technical, support-related, protection… all with one main challenge: Time-To-Market. Such initiatives are crucial since they represent a basis for a constructive relationship that may be built between VC Providers and VC Users. But it will take time for practitioners to adopt such standards, which have to be internalized in corporate cultures, adapted within design flows, and which have to face fears about quality issues. The VC business is a fledging niche that will remain unstable due to its huge need for improvement of the technical and business relationships.

The Time-To-Market challenge requires from a VC Provider an efficient and convincing offering, with credible answers to all questions, plus the ability to quickly tune this offering to account for the constraints of SoC Integration: design methodology, decision processes within the organization… so as to turn the design-in process into a really cooperative business model.

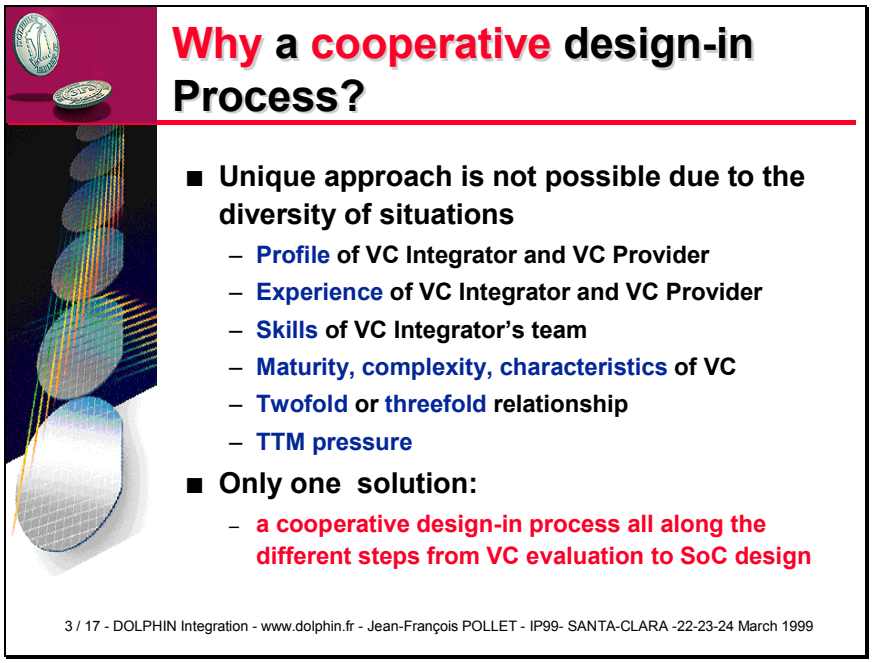
Such a Design-in process at Dolphin is under continuous reassessment for improvements based on a particularly rich experience in mixed signal Virtual Components. The risk of such a dynamic reassessment is to make every step blurry, while our quality-obsessed process entails firstly that a higher Index of Quality, i.e. IQ, is requested of the VC for the Design-in process.



Overview

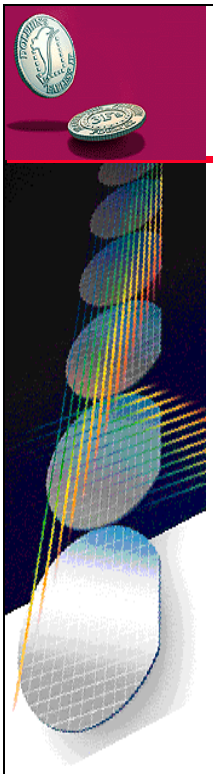
- Why a design-in cooperative process?
- The different steps from SIP to SoC
  - VC evaluation phase
  - Business agreement
  - ECOs & process migrations
  - Integration in design flow
  - Support
- Conclusions

In a first step, I will explain why such a design-in process is usefull between a VC provider and a VC integrator.
Then, we will examine the different steps of the relationship starting from the evaluation phase of the VC by the integrator, including the ECO, continuing by the establishment and discussion of a business agreement and last, but not least I will describe what we consider as one of the most important issue, the support VC supplier has to provide to Integrators.
It will be then time for conclusions.



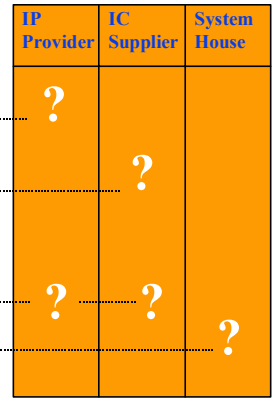
How to summarize the diversity of VC offering and the diversity of SoC requirements?
An exhaustive list of this diversity is impossible to establish, let us look at only a few of them and explain which impact they may have on the relationship between VC Provider and VC User, and consequently why a cooperative Design-in process is the only solution towards success:
- The profile of the VC User intending to buy the VC: small or large Corporation, System House or Semiconductor Manufacturer, Foundry… Each of these corporate types will have its own habits and own requirements: specific business models when they exist, specific design flow, specific tools, preference as to working with hard VCs versus soft VCs…
- The experience and maturity of the SoC Integrator intending to buy the VC: Companies new to this business – as most are - need to be trained while they may even not understand the differences between VC Providers and ASIC design centers. Some are under the influence of past experiences in using VC – whether bad or nice - strongly influencing the way they want to do business.
- The skills of the integrator's team intending to buy the VC in the domain it addresses: the respective responsibilities of the VC Provider and VC Users have to be explained and clarified especially regarding system know-how; e.g. a company with no skills in mixed signal design will have difficulty understanding whether specifications of a specific ADC fulfill the needs of a given application.
- The nature of the VC Provider intending to sell the VC: small or large Company. A small Company is often more flexible and reactive, but may be perceived as more fragile or fuzzy.
- The maturity, complexity and characteristics of the VC to be sold: - Is it a new product or product with a success story? - Does it require custom adaptions for the targeted application? - Does it require a retargeting work toward a specific process? - Does it require an evaluation through a test circuit?
- The relationship is sometimes twofold, sometimes threefold, depending on whether the SoC Integrator is an IC supplier (as for ASSP) or an ASIC designer using the VC as a component within a library provided by the IC supplier or by some foundry.
- Last but not least, the time-to-market pressure: this is definition itself of the market addressed by any VC. In such a case, a VC User may not have time to look in depth into the different aspects (technical, legal and commercial) of the relationship with the VC Provider. To efficiently address this issue, the VC Provider has to offer ready-to-use technical, commercial and legal proposals.

Every step of the relationship between VC Provider and SoC Integrator will be influenced by such factors. It may result in business relations and in a Design-in process totally different, covering a wide range of solutions. For instance, pricing issues may cover cases ranging from one-shot deals with up-front payment for a hardware VC, decided within some weeks, up to a deal for multiple uses, mixing royalties and up-front payment after more than one year of negotiation, plus requiring delivery of a soft VC plus continuous support during two years.
It entails the best solution for one customer is certainly different from another's and has to be built through an interactive and cooperative process. Such a process must be conceived at the start of the evaluation phase.



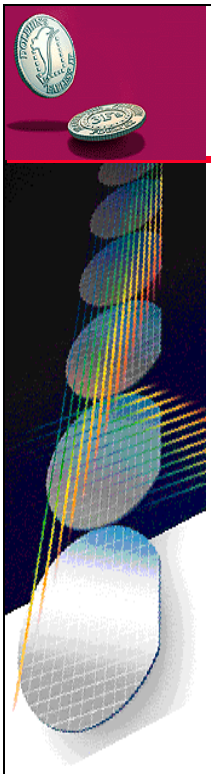
Example of diversity

- Integration of VC into a SoC
  - for ASSP: 2 partners
    - IP Provider
    - IC Supplier
  - for ASIC: 3 partners
    - same partners plus
    - System-House



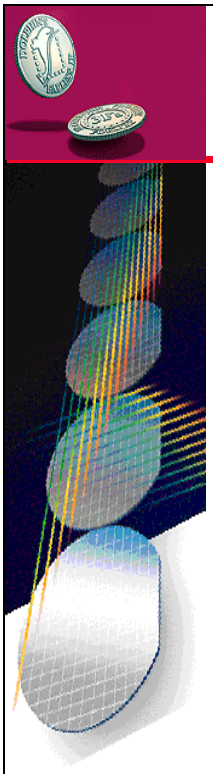
➥ Business model is different

Just have a look at one of the examples of this diversity. The case when relation is twofold, envolving a VC provider and an ASSP supplier, compared to the case when the relation is threefold, envolving the same VC provider an ASIC supplier and also a third party, typically a system house. Typically in the third case, the ASIC supplier will buy a VC to put it in its macrofunctions library. The work to achieve this goal is much more complex than the work to do for the usage of the same VC in an ASSP. Furthermore, in the case of a threefold relationship, the VC provider has to supply different kinds of support:
- support to application designers of the ASIC suppliers
- support to final user, usually the deisgner of the system house
We understand easily that the relations, from technical and business points of views cannot be the same.



Cooperative Design-in Process all along the different steps of the relationship

- Step#1: VC evaluation
  - Data exchanges
  - Cooperative analyse
  - Review of ECOs
- Step#2: Business agreement
  - Deliverables and schedule
  - License agreement
- Step#3: ECO implementation / Migration
- Step#4: Integration in design flow
- Step#5: Support



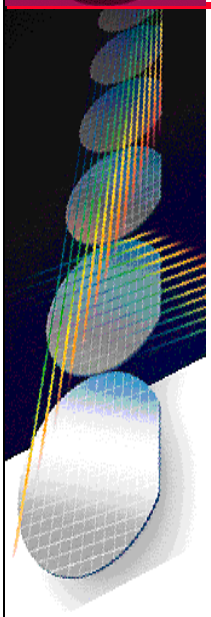
Step#1: VC evaluation-1

- **Purpose of the evaluation: does the VC fit the customer 's requirements?**
- **Free data on the web or upon request**
  - **Data sheet, promotion sheet**
  - **Application notes,**
  - **Patent descriptions,**
  - **Demonstrations…**
  - **Principles of Support Engineering**

➥ **Necessary but not sufficient!**

The purpose of the evaluation is…
The VC business requires operating on a worldwide scale. Web sites, research engines enable designers anywhere in the world to get quick access to some VC and some data about its VC Provider. It usually remains difficult for the VC User to sense the adequation of the described VC and its SoC application, mainly for two reasons: on the one hand, the VC Provider hesitates to put a lot of data on the Web for fear of loosing confidentiality and know-how; on the other hand the SoC Integrator may not know precisely what he needs as a function, either because the detailed specifications of the SoC are not yet known, or because he has no expertise about the function processed by the VC; in the latter case, the VC User does not really understand the differences between competitive offers.
An evaluation phase of the VC then is crucial, together with a close relationship with the VC Provider: or possibly a partnership!
The evaluation phase may be quite brief, and should certainly be shortened in the future due to the increasing pressure of time-to-market. Consequently VC Providers must be able to provide substantial and relevant data to the prospect and reciprocally.

Step #1: VC Evaluation-2

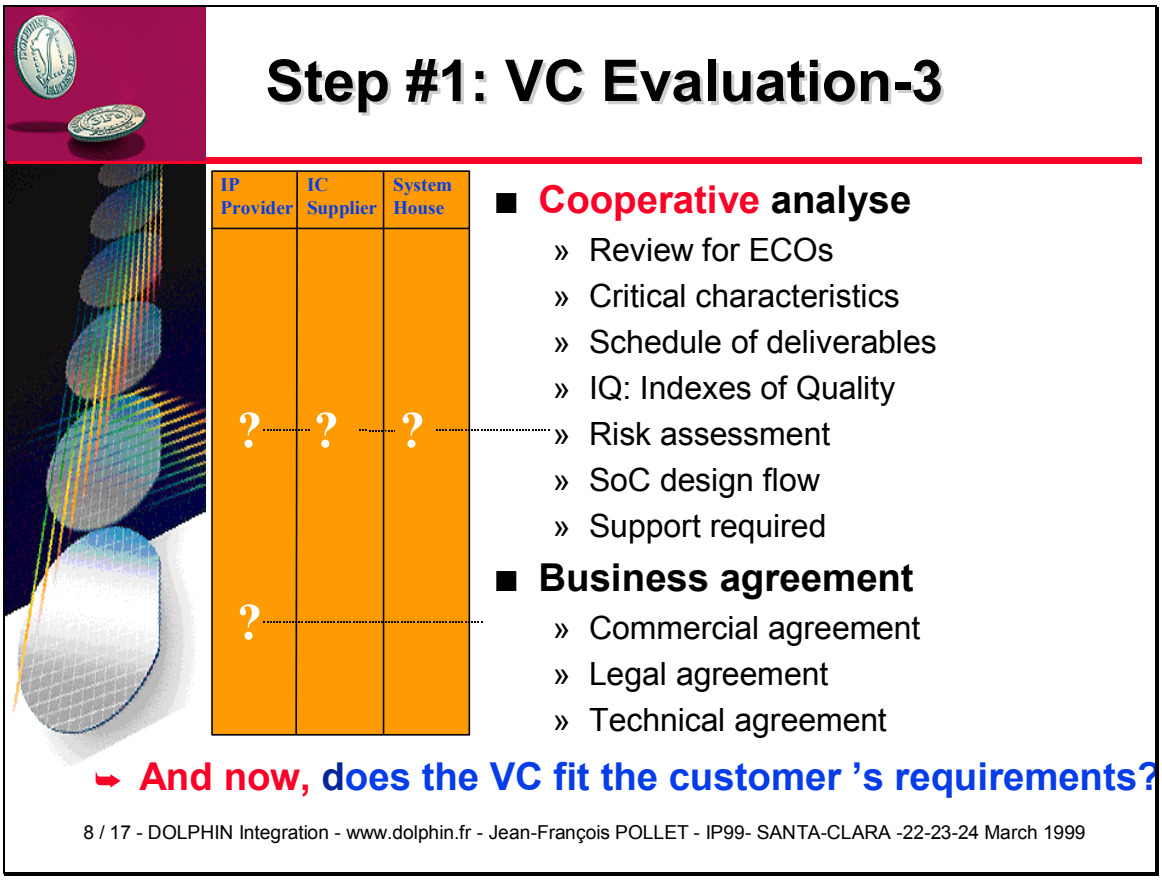


IP Provider	IC Supplier	System House
?		
?		
	?	
	?	?
?		

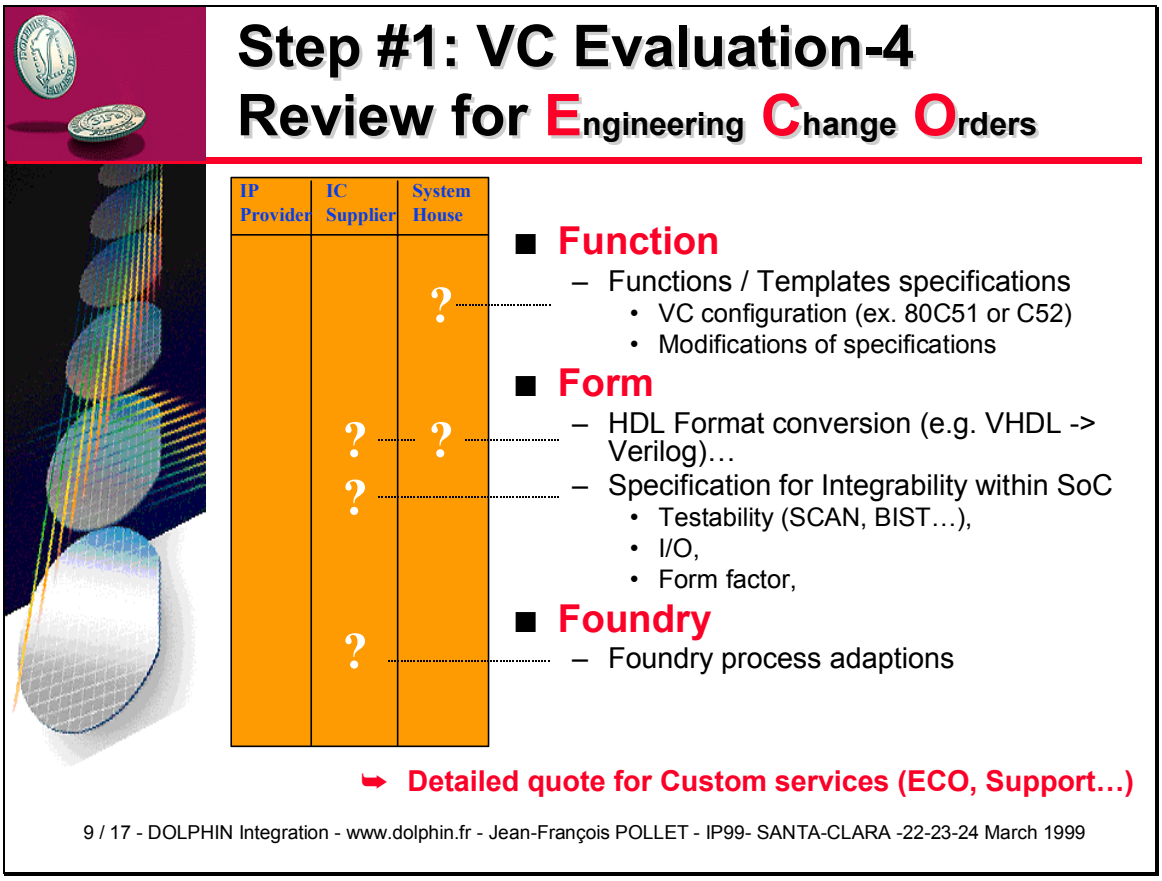
- **True ISO-9001 procedure**
- **Non Disclosure Agreement for:**
  - » VC detailed specifications, flexibility, programmability, portability
  - » Availibility of demonstrators: simulation kit, eval board, demo, characterization results, prototypes…
  - » Process data
  - » SoC specifications
- **EValuation Agreement:**
  - » Simulation model, eval board…

➥ **Does the VC fit the customer 's requirements?**

VC Providers need to understand the user application; VC Users need to understand at proper depth the offering of a VC Provider. A mutual NDA is therefore mandatory at this stage.
We shall never tell it with enough strength: such an evaluation phase has to be performed per an ISO-9001 procedure, since success of the whole Design-in project depends on accuracy and professionalism in the relationship between the two parties at this stage. Main interactions between VC Providers and VC Users are summarized on the slide. Exhaustivity is not attempted. Supplying any data described in this table, by either party to the other, requires acknowledgements, comments and formal agreements, or requests for modifications.
The evaluation process may be very brief or quite long depending on the factors described previously. Our own experiences vary between one week and one year!!
Lire le slide
Information on the targeted process is required by the VC Provider to check whether the VC may fulfill the specifications within this process. Such data are mandatory for a “hard“ VC.

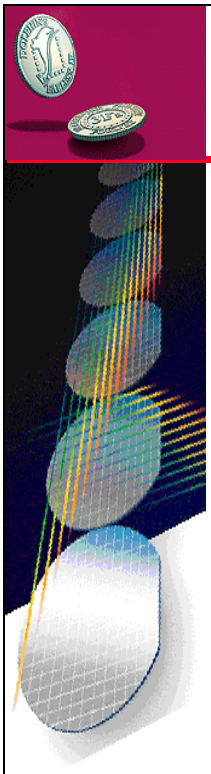


In a following step of the evaluation phase, the parties have to enter a cooperative anayse covering variuous aspects like:
… lire et commenter le slide..
Critical characteristics subsume speed, power consumption, silicon area, noise, or any feature intrinsically critical, or critical with respect to the targeted process.
Indexes of Quality: they mean the IQ of the VC Provider's design process, summarizing all VC checks. Criteria range from check-up exhaustivity (Testbenches, simulations…), to characterization coverage of prototypes, and testability of the VC…
Risk evaluation: both parties have to clarify and quantify the risks of the Design-in project, and the nature of such risks: technical, schedule… so as to be able to put in place a quality-assurance process for reducing risks to a minimum.
Most of the items described are based on exchanges by phone, email, fax or face-to-face meeting. Additionally, the VC User may manage deeper evaluation, if time allows:
On silicon demonstrators when practicable, and if the user has the right tools for evaluation,
On models: thanks to its mixed-signal simulator SMASH, Dolphin is able to provide demos on the Web using encrypted simulation models of the VCs. In the future, standards like the Open Modeling Interface (OMI) currently in discussion for an IEEE standard will help protect models for easier VC evaluation and shall enable truly Virtual Testing.
Reference to existing or pending standards like specifications promoted by VSIA is helpful and should speed-up cooperation between companies having adopted them.
Such a cooperative analyse is particularly important for complex functions, encompassing a lot of working modes or for mixed signal VCs.
The question asked at the beginning of this phase must have now an answer.



The question here is what has the VC provider to do for having an offer in accordance with the requirements of the VC Integrator. What changes, if any, compared to the original product, have to be implemented?
Two kinds of changes:
1 - Modifications of specifications: some functionnality or some characteristics may have to be introduced to fit the applications needs
2 - Modifications for tuning the product to a process or a specific design flow
Both may include:
- Modifications of design and of layout in case of hard VC
- retargetting toward a new process
If modifications have to be done, a description of the methodology has to be put in place, with a common analyse of the risks, if any, due to such modifications

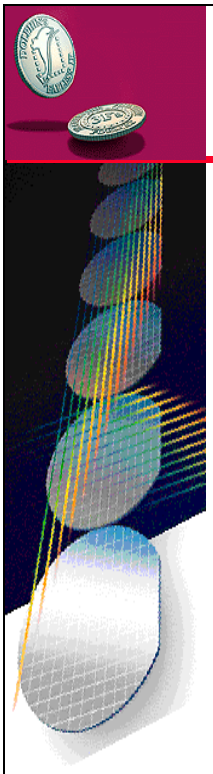
Once again, a strong cooperation is needed between provider and integrator to be sure that nothing will remain unclear.
At the end of this evaluation phase, a complete proposal can be done by the VC provider.



Step #2: Business Agreement

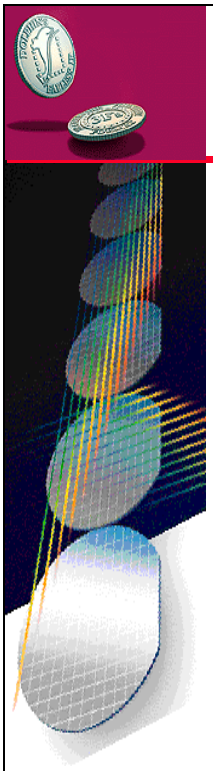
- **Technical appendix with deliverables and schedule**
- **License Agreement**
- **Terms and Conditions**
- **Support Agreement**
  - **Trust**
  - **Yield**
  - **Training**
  - **Delegation…**

What will typically contain a Business Agreement
- a technical appendix, summerizing the specifications of the VC, ECOs which have been agreed upon, content and schedule of deliverables,
- a legal agreement I will described in details in some minutes
- the terms and conditions detailing the schedule and amount of invoices, usuallyt associated to deliverables. A lot of various business models exist, based on fixed fees, royalties and a mix of both. But it is not discussed in this presentation
- finally, the support, we consider as a very important issue, because the necessity of support is sometimes completely ignored by integrators, and in any case underestimated



Step #2: Deliverables and schedule

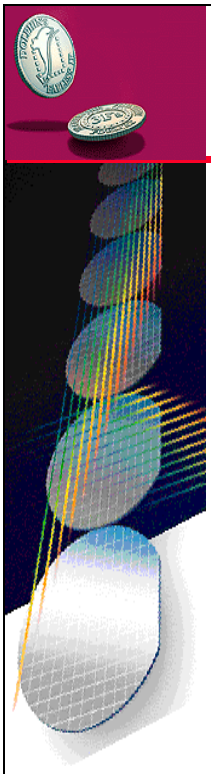
- **Deliverables**
  - **Logic soft VC**
    - Specifications
    - HDL description
    - Testbench for functionnal simulation & virtual test
    - Synthesis scripts
    - User's Guide
    - Behavioral model
  - **Specific for Embedded memory compiler**
    - Development kit (for ROM programming)
    - Scripts for integration under frameworks
    - Additional Output views (Abstracts, Schematics, Synthesis model…)
    - Front-end generator (dissociated from back-end)
  - **Specific for Mixed Signal VC**
    - Spice netlist
    - GDSII format database for analog functions
    - Evaluation board and test specifications
    - REPACK



Step #2: License agreement: some of the issues...

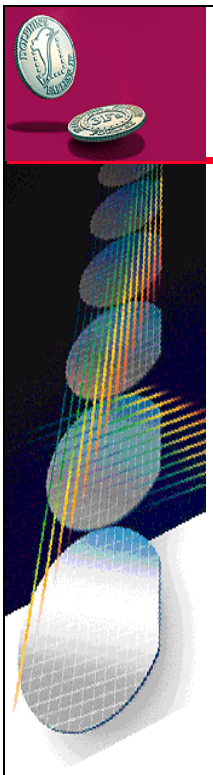
- **Grant**
  - description of the Licenser/Licensee roles and rights
- **Warranty**
  - commitment on deliverables
  - trust agreement
  - design-defect fixing and upgrades
  - assistance in case of claim for rights infringments
- **Derivative works**
  - modifications of the V.C. can be made either by Licenser for Licensee or by Licensee
  - proprietary rights remain Licenser's

Discussions around the license agreement often take a long time, especially within large corporations. This explains why a typical license agreement has to be presented by the VC Provider at the start of the discussion. We had several experiences where the license agreement had been signed by the parties at the same time as the delivery of the VC, even after a development time of 3 months.
What kind of questions must the license agreement deal with? - some of them are mentionned on the slide and we may add others like:
-Company and Territory: - Which Company or Division in the Company will benefit from the agreement? - Are subsidiaries concerned or not?… - What happens when the licensee acquires a third party or is acquired by another?
-Grants: - What are granted versus non-granted rights and for what product? - What about VC subsets?
-Warranty: - Duration? - What is covered?
-Trust Agreement: - What happens if design defects are found in VC deliverables, depending on when they appear? - Who shall bear the burden to prove, and how, that defects are coming from the deliverables and not from usage which has been made of them? - What happens if design defects are found to be due to the VC during the production phase of a SoC using it?
-Patents: - What happen in case of patent infringement? – Or simply under unfair litigation?
-Derivative works: definition, ownership, associated grants and trust agreement?
-Updates: - How are they managed? - Associated grants and trust agreement?
-Applicable law and court of jurisdiction in case of conflict?…



Step #3: ECO implementation

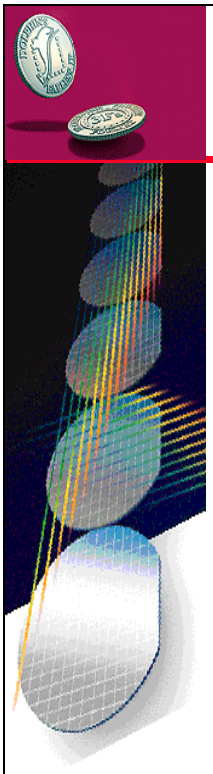
- Wide range of reasons for ECO implementation a la ISO9001: process of design/verification and delivery/acceptance to be put in place
- Testbench / REPACK enhancement by different designers from ECO implementation
- Retargeting process (Mixed Signal & Embedded Memory)
- Verifications
  - **Testbench for logic VC**
  - **REPACK for mixed signal Vc and for embedded memory generators**
- Risk control



Step #4: VC Integration in SoC Integrator design flow

- More accurate the VC evaluation, more efficient the VC integration
  - constraints to respect / design flow
- Formal acceptance of deliverables, usual and issued from ECO:
  - you still have some time to save!
- Training and support are required for VC integration
  - Hard to imagine the imagination of an integrator
  - Exhaustive documentation is not the answer

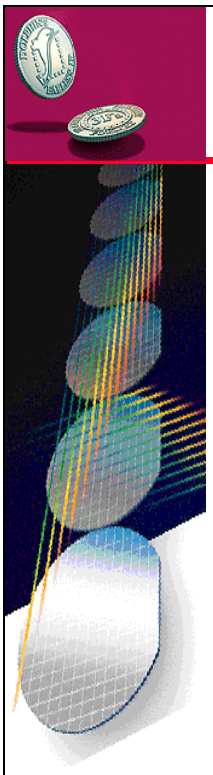
One of the key issues for the technical agreement is the method for inserting the VC into the design flow of the VC User. VC Users use design flows and tools looking similar when considered at a high level, but showing key differences through any zoom effect. Significant differences in requirements and internal rules appear for documentation, testability, naming conventions, specific constraints for hardware blocks… General discussions about the use of such HDL or about the availability of such scripts are not enough. Highly skilled designers must spend time detailing the whole method and custom constraints to be taken into account.
Once again, the constraints to take nto account for the insertion in a library will not the same as the constraints for th eusage in a single ASSP.
Furthermore, complexity of this issue will also highly depend on complexity of the VC itself: delivery of a UART VC in a HDL format will not be managed in the same way as that of a complex mixed signal circuit which shall involve design and implementation of a test circuit, specification and design of a characterization board, plus measurements on prototypes…
Another item to mention is that deliveries coming from VC provider always have to be accepted formally, either by running simulations or different checkin like DRC, LVS and so ne. The reason for that is to check that no misunderstanding of data bases format or content is remaining. Doing such acceptance quickly after delivery allow to save time in the whole project.
To introduce the next issue, I will finish by the necessity of training and support, especially for complex VC. A detailed documentation is absolutely necessary but experience shows that even with a good documentation, additionnal support is required for a lot of reasons:
- complex VC may imply complex documentation, difficult to manage by a user who will prefer to have a direct support than spending time searching in the documentation
- VC users have a lot of imagination and sometimes want to use the VC in unspecified modes, requiring advices from the provider



Step #5: SUPPORT

- System on PCB needs support from IC vendors
- Usage of complex software tools needs support from EDA vendors
- Issue amplified for System on Chip design
  - hard and soft VCs
  - Lack of standards
- Level of support is different for an UART, a JPEG a µC, a AMS codec

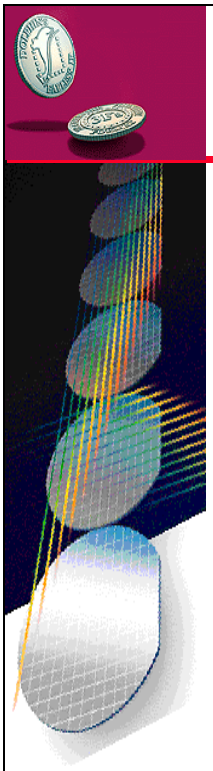
Who would deny it today? The support is a key factor for the success of a SoC design.
In the same way a designer of a system on PCB requires some support from. an application engineer for the usage of such real component coming from. one vendor, in the same way, the designer of a SoC will need support to insert the VC in his chip.
Clearly, the SoC designer will not ask for the same support for a simple function like an UART and for a complex function like a JPEG , a micorprocessor core or a mixed signal codec.
It means that requiring support is a natural issue.
But there is a significant difference between PCB and SoC
What the industry has normalized since decades in the PCB world, allowing today a designer using on the same board chips coming from. different vendors, the semi-conductor industry has not yet succeded in doing it. The time certainly will come when VC in a SoC will be use as RC on a board but in the mean time, a high level of support is required.



Step #5: SUPPORT

- The question(s)? various needs
- The answer(s)? flexibility
  - Training
  - Delegation for design services
  - Support to customer 's customers
  - Updates and bug fixing
  - Yield support during the production phase

We distinguish several kinds of support, which may be provided in different ways:
-By the presence of one or several engineers from the VC Provider at the customer's site; it may be the case for training sessions, design-in support necessary for initial integration of some VC into a specific design flow, or for maintaining the VC compatible throughout the evolution of the design flow. It has to be performed by a designer with deep knowledge of the VC, in cooperation with a designer having thorough knowledge of the design flow.
-By subcontract design to the VC Provider; work being most of the time performed at the VC Provider's site. It may be the case for ECO's (Engineering Change Orders) required by the VC User in case of a new application, and for design support for maintaining the VC compatible throughout evolutions of the process design rules (in case of a hard VC).
-By hot-fax, or nowadays "hot-email". It is often the case:
- for interfacing with third parties' users; e.g. when the VC has been delivered for augmenting the library of an ASIC supplier. Customers of this ASIC supplier are the real end-users of the VC for their SoC integration. They need support for understanding the VC and how to interface with it…
-process and product engineering support during production for dealing with yield issues. Adequate solutions have to be discussed and found with the VC User. TTM pressure requires that support must be very effective with a high reactivity. Recent experiences at Dolphin have shown that support through the Web may be really efficient and successfully experienced for design support and yield support during the production phase.



CONCLUSION

- TTM is the major goal of SoC market
  - Reactivity, Quality and Flexibility are the main factors
- VC providers must
  - Adhere to standards
  - Offer ready-to-use deliverables
  - Focus on the IQ of IP (quality)
  - Strive to remain flexible
- SoC designers must
  - Specify clearly their technical and business constraints
- The road to success?

  a cooperative design-in process

When Time-to-Market becomes the main rule of any business, reactivity, quality and flexibility are the main values driving to its success.
As an experimented VC Provider selling various kinds of VC to diverse kinds of customers, below are our major recommendations for actors in this emerging market. We first address the community of VC providers, often independent SME's.
Have a clear and basic offering with ready-to-use proposals encompassing technical, legal and commercial issues, but be prepared to be flexible; also think that you may be in competition with third parties or be one VC providers among several for the same SoC, and your customer has to spend a minimum time to manage each deliverable and each provider.
For the technical issues, adopt the specifications of VSIA, at least a subset. Also consider that a high level of documentation will be required by any customer.
Explain the design quality procedures you are following to prove a high IQ for your VC.
Spend time explaining your business model simultaneously to technical, marketing and purchasing people for a clear understanding of the impact of such or such decision. Dually, spend time understanding the internal culture and design flow of your customer.
Detail your support policy: support and reactivity are the major advantages of SME's.

For the SoC integrators now, our major recommendation is to actively cooperate with the VC providers. The more transparent and accurate they may be about their needs, the more efficient the relationship shall be, with the best chance of success. Deliver a set of requirements to VC providers as soon as possible:
requirements (mandatory or recommended) for specifications and deliverables,
business guidelines with realistic expected time schedule, risk, budget, decision process.