Mixed Signal Virtual Components
Meeting the challenge of Design Reuse and Time-To-Market thanks to
a flexible high resolution ADC generator

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Overview of the presentation

- Introduction: **Design Reuse** and **Time-To-Market**, a challenge for **Mixed Signal** VCs
- **ADMIR** or how to answer such a challenge with a high resolution ADC generator
  - Main characteristics and **flexibilities** for various application requirements
  - The **generator** approach enabling these flexibilities
  - What is delivered to a customer?
  - How Dolphin may **retarget** to different CMOS processes **within a few weeks**
  - **Efficiency** of such a retargeting (performances and cost)
- Conclusion and trends

Introduction

- **Design Reuse and Time-To-Market**, a real challenge for **Mixed Signal** Virtual Components
  - Users often (always?) need a solution « slightly » different from mixed signal macrocells available (sometimes) in a library.
  - In analog, the difference between a completely new design and modifications of an existing one may be very thin!
  - Users often (always?) need the VC in a process requiring a **retargeting work**. In analog, such a retargeting work may consume a lot of human and computer ressources and the original designer is now working on other projects!
  - When building a **System On Chip**, users always expect receiving the analog VC data base **simultaneously with the rest of the logical design**, within a **very short time**
- How to answer such challenge?

Case-study

- How to cover a wide range of characteristics for an ADC with following features?
  - Delivered as a Virtual Component **within a short time**
  - **Retargetable towards any submicron 3V CMOS process, analog or digital within a short time**
  - Able to cover **various characteristics** like:
    - Number of input channels between 1 and 12
    - For each channel, a **resolution from 10 to 16 bits** with a sampling frequency from DC to 50 kHz
    - Differential or single-ended inputs
    - Single power supply voltage 3V
    - And many other features…

The Dolphin response: ADMIR

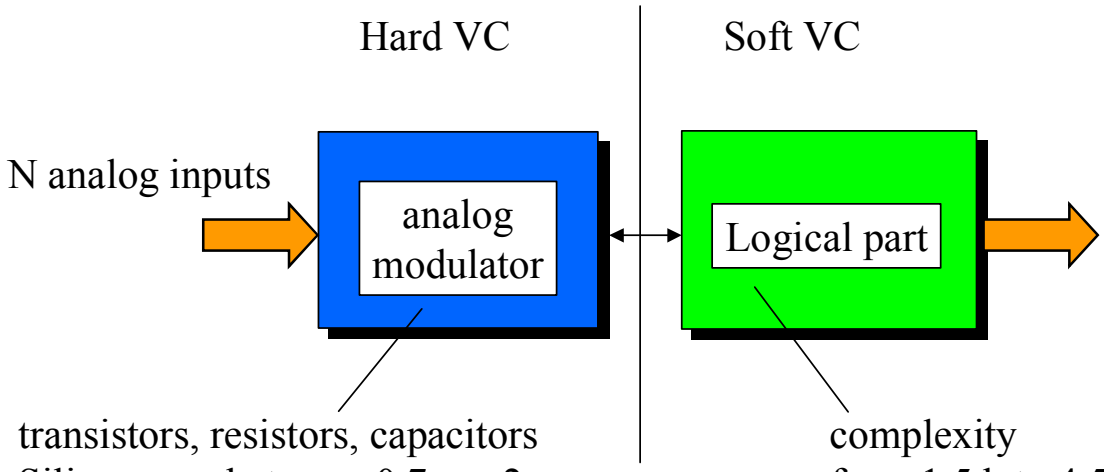
- Based on a **generator** approach:
  - The user specifies its needs by answering questions through a user interface
  - The generator evaluates and proposes different solutions
  - The generator generates the chosen solution, a **« cut »,** optimized for the required performances and provides ready-to-use deliverables of this **cut**
- Based on an efficient **retargeting methodology** which guarantees short schedule for **porting** in a new technological CMOS process
- This work has been sponsored by the European Community: Esprit project NAOMI

Réponses du générateur

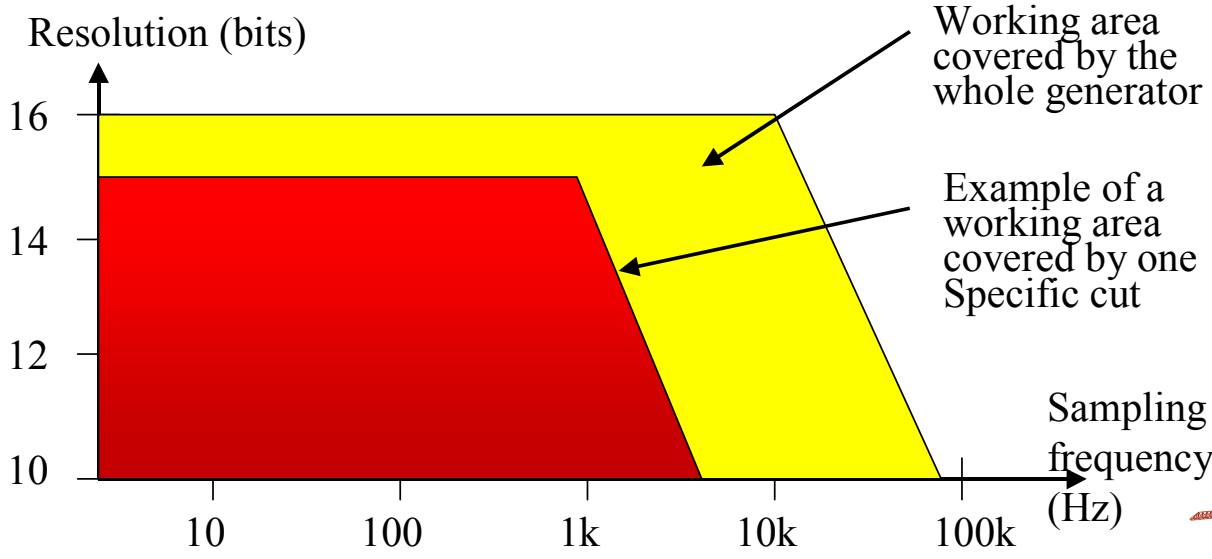
silicon area of the analog part
estimated number of gates of the digital part
frequency of the main clock per channel
actual table for Ncodes, DNL, INL, … and DECIM value
power consumption

ADMIR

A « cut » is a mixed signal VC



ADMIR - working area of the generator



ADMIR
Flexibilities and main features

- Flexibilities
  - The number of analog input channels = N between 1 and 12
  - For each analog input: fixed or programmable
  - For fixed inputs: #codes, INL, DNL, Fs, choice between differential / single ended,
  - For programmable inputs: #codes, INL, DNL, Fs, the choice between differential and single-ended remains possible during the working mode
  - The use of internal or external voltage reference
  - stand-by, shut down and normal modes
  - zero tuning mode for an offset-cancellation of each channel separately
- Application fields: Data acquisition, measurement, sensors…

ADMIR - Interface Dolphin-Customer

- The Customer describes to Dolphin the features of a required ADC by answering a set of questions
- Dolphin runs the generator and proposes the possible cuts and associated data sheets
- After agreement on the right data-sheet, Dolphin generates the selected cut and provides the deliverables to the customer

ADMIR
Deliverables for a cut

- In accordance with **VSIA** specifications
- For the logical part
  - Synthesizable Verilog RTL Code
  - Verilog Testbench and test vectors
- For the analog part
  - Abstract for Place and Route
  - GDSII data base including all mask layers, in accordance with the targeted process design rules
  - Spice Netlist
  - Analog behavioral model (ABCD) on request
- For both
  - Datasheet and detailed specifications
  - User's guide

ADMIR: benefits for the Customer

- Enables to cover a **wide range of customers needs** thanks to a lot of flexibilities
- Satisfies both **Design-Reuse** and **Time-To-Market** criteria
- a specific cut is available **within some minutes** in an already predifined process
- What about the retargeting in a new process?
  - ADMIR generator has been designed for easy retargeting towards any submicron 3V process
  - Either the whole generator or a single cut may be retargeted
  - In any case, the deliverables will be possible within a short delay, compatible with usual requirements from customers

ADMIR Retargeting: how is the generator built?

- Logical part generation
  - ADMIR generators uses three different RTL parametrized models, associated to the analog modulators
  - When the generators selects one cut, one RTL model is chosen
- Retargeting the logical part does not need additional design work thanks to the use of a RTL synthesizable model in HDL
- Data sheet generation
  - ADMIR generator uses a « meta » data sheet and fills the values when the cut is selected; values are issued from the simulation files
- Retargeting the data sheet only requires having done the retargeting of analog part

ADMIR Retargeting: how is the generator built?

- Analog part generation
  - ADMIR Generator uses 13 different basic hard cells: AOP, comparators, bandgap, phase generators
  - Basic cells are used by 6 different hard modulators
  - When the generator selects one cut, one modulator is chosen
  - An Analog Test Bench is associated with each cell and each modulator
    - Simulation configuration
    - Stimuli
    - Data sheet with parameters to extract
- Analog part retargeting = schematics retargeting + layout retargeting

ADMIRxy - Layout of the analog part

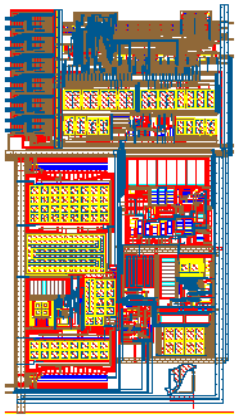
ADMIR-11

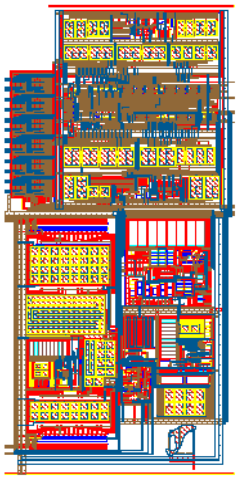
Area: 0.73 mm²

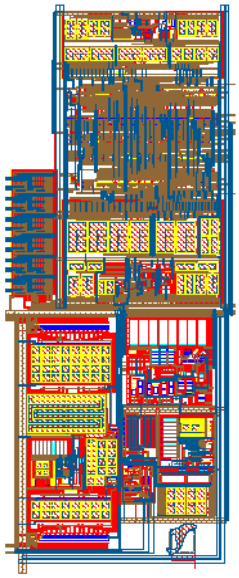
ADMIR-21

Area: 0.84 mm²

ADMIR-31 Area: 1.02 mm²







Includes

REFERENCE
+BIAS

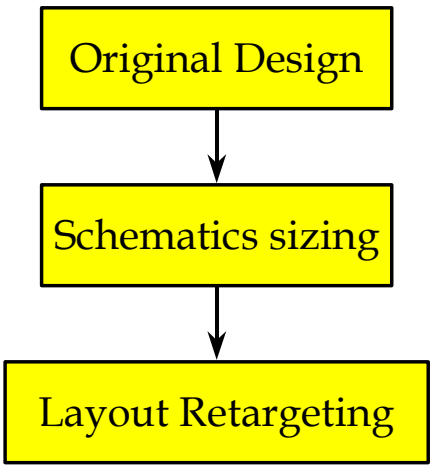
0.42 mm²

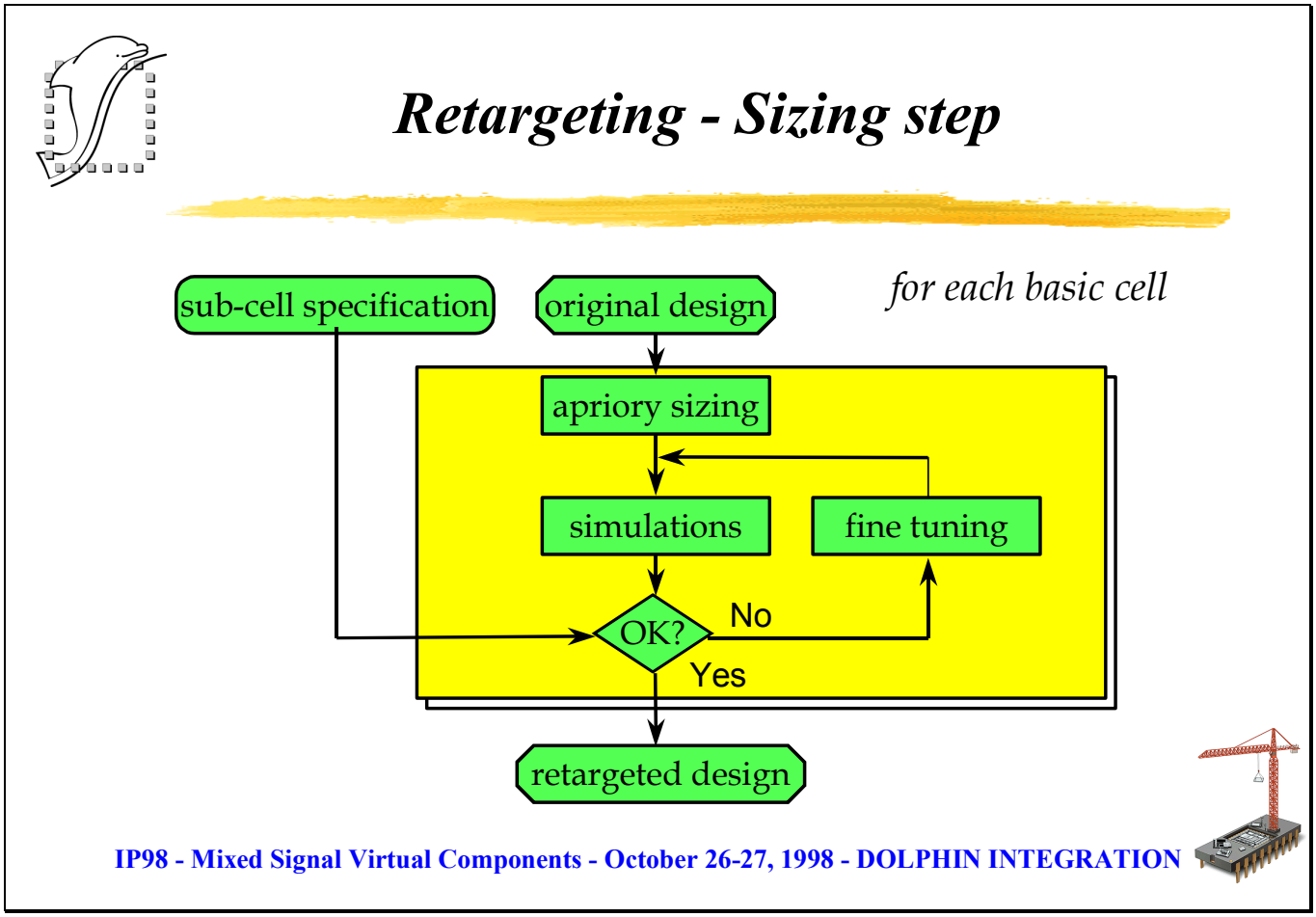
Retargeting methodology

- same schematic
- similar specifications

- a priori sizing
- fine tuning

- semi-automatic layout porting
- manual correction





Analog test bench
Robust design rules including:
use of in-house generic device models with a wide variation range on key parameters (threshold, mobility, oxyde thickness)
use of robust schematics avoiding process dependant effects
rules for the layout and visual control for symetries, mismatch influences, power supplies lines, critical signals crossing, isolation between analog and digital

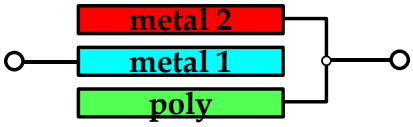
hierarchical approach

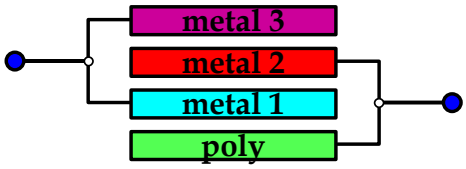
by design the global specification is met when every sub-cells specification is met

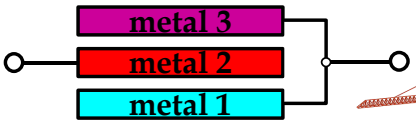
A priori sizing
depends on:
the sub-cell itself
the gap between the initial and final technologie
the gap between the initial and final specification
usually:
systematic sizing on digital part (phase generator, decoder, ...)
specific sizing on analog cells (output stage of the OAP, switchs, capacitors, ...)

Sizing -example of the capacitors

- **Process A- 0.5 µm**
  poly/m1/m2 sandwich capacitor
  => 126 ± 14 aF/µm² (parasitic: 68%)
- **Process B- 0.35 µm**
  poly/m1/m2/m3 sandwich capacitor
  => 120 ± 13 aF/µm² (parasitic: 76%)
  => sizing coefficient: 1.05
- **Process C- 0.35 µm**
  m1/m2/m3 sandwich capacitor
  => 126 ± 43 aF/µm² (parasitic: 30%)
  => sizing coefficient: 1



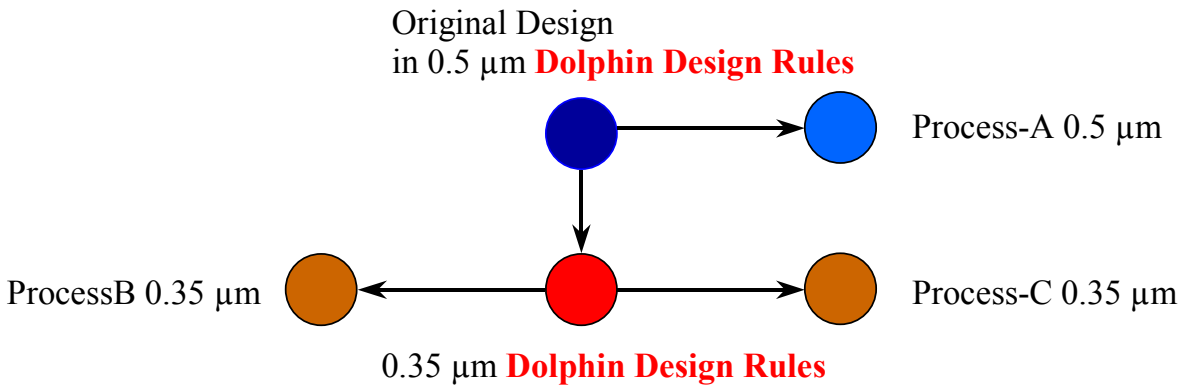




Retargeting - Layout

Mix of **vertical** and **horizontal** retargeting

- vertical retargeting uses systematic sizing of some devices
- horizontal retargeting uses specific sizing



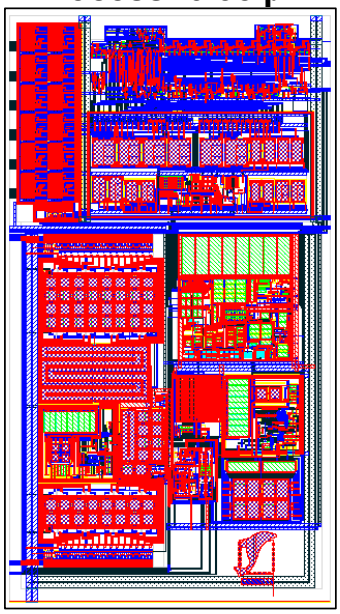
hierarchical approach
start from exixting layout
graphic resizing with ***GDS Strata™***
manual finishing
use our own graphic rules for a set of technologies to simplify the retargeting

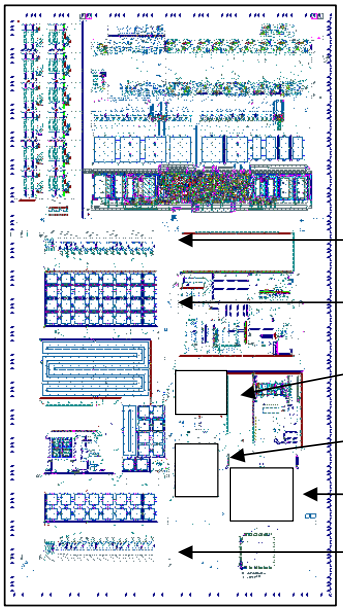
Layout retargeting

Process: 0.35 µm

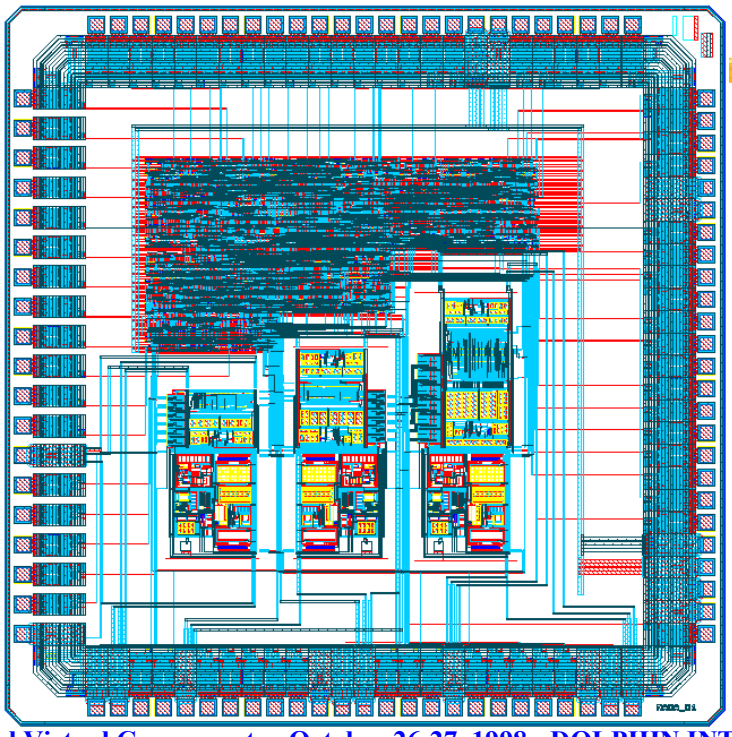
Difference with 0.5 µm process

Same area: 0.73 mm²





ADMIR Test circuit



Retargeting - efficiency / performance

	CODAN31 Process-A 0.5 µm	CODAN31 Process-B 0.35 µm	UNIT
Maximum power consumption	**2.1**	**2**	**mA**
Area	**1**	**1**	**mm^2**
Signal to Noise Ratio			
differential mode			
12 bits resolution	**70**	**70**	**dB**
14 bits resolution	**80**	**80**	**dB**
single ended mode			
12 bits resolution	**70**	**70**	**dB**
14 bits resolution	**82**	**81**	**dB**
Maximum output sampling frequency			
differential mode			
12 bits resolution	**26**	**26**	**kHz**
14 bits resolution	**12**	**11**	**kHz**
single ended mode			
12 bits resolution	**27**	**27**	**kHz**
14 bits resolution	**12**	**12**	**kHz**

Retargeting - efficiency / performance

	Process-A 0.5 µm			Process-B 0.35 µm			
	OPA1	OPA3	OPA4	OPA1	OPA3	OPA4	UNIT
minimum open loop gain	100	110	100	110	110	110	dB
minimum gain band-with differential mode single ended mode	 28 48	 35 44	 25 48	 33 59	 31 39	 26 63	 MHz MHz
maximum power consumption	370	920	1100	480	880	960	µA
maximum equivalent input noise	342	336	230	580	492	363	μV_{rms}
maximum settling time for a 4V step to reach a given final error in differential 0mode final error : 480µV (for 12 bits resolution) final error : 120µV (for 14 bits resolution)	 80 103	 65 ~	 100 110	 81 104	 78 ~	 104 120	 ns ns
maximum settling time for a 2V step to reach a given final error in single ended mode final error : 240µV (for 12 bits resolution) final error : 60µV (for 14 bits resolution)	 75 87	 75 ~	 95 110	 75 92	 73 ~	 98 97	 ns ns

~ not reached

Retargeting - efficiency / cost and delivery time

Analog part design

		One cut				Whole generator		
Cost and delivery time	**CAE cost** man*weeks	**CAD cost** man*weeks	**Overall cost** man*weeks	**Delivery time** weeks	**CAE cost** man*weeks	**CAD cost** man*weeks	**Overall cost** man*weeks	**Delivery time** weeks
First design	15	8	23	20	80	32	112	60
First retargeting	4	4	8	6	20	24	44	26
Second retargeting	4	3	7	5	20	8	28	18

Conclusions and trends

- Thanks to the Dolphin know-how in mixed-signal design:
  - We have proposed a **new concept: generator of Virtual Components**, for better answering Customer expectations: **various needs and Time-To-Market**
  - We have demonstrated the **efficiency** of **retargeting** methodology to **shorten design cycles**
  - **ADMIR** features may be extended: decreasing power consumption, increasing sampling frequency or resolution…
- The generator concept may also be applied to other mixed signal VCs like PLLs, DACs, Codecs…
- The continuous progress in retargeting methodology will more and more reduce the Time-To-Market for mixed signal VCs and extend their use in SOC design.