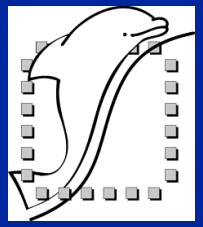
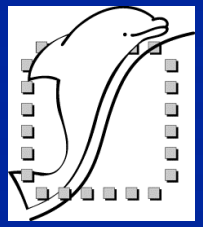


Overview of the presentation

- Introduction
- Two examples of Mixed Signal Virtual Components
  - COLINE, Analog Front End including a delta-sigma CODEC for fax, modem and audio applications
  - LPCOD, Ultra low-power CODEC
- Mixed Signal Virtual Components: deliverables
- Mixed Signal Virtual Components: design methodology
- Conclusion and trends

INTRODUCTION

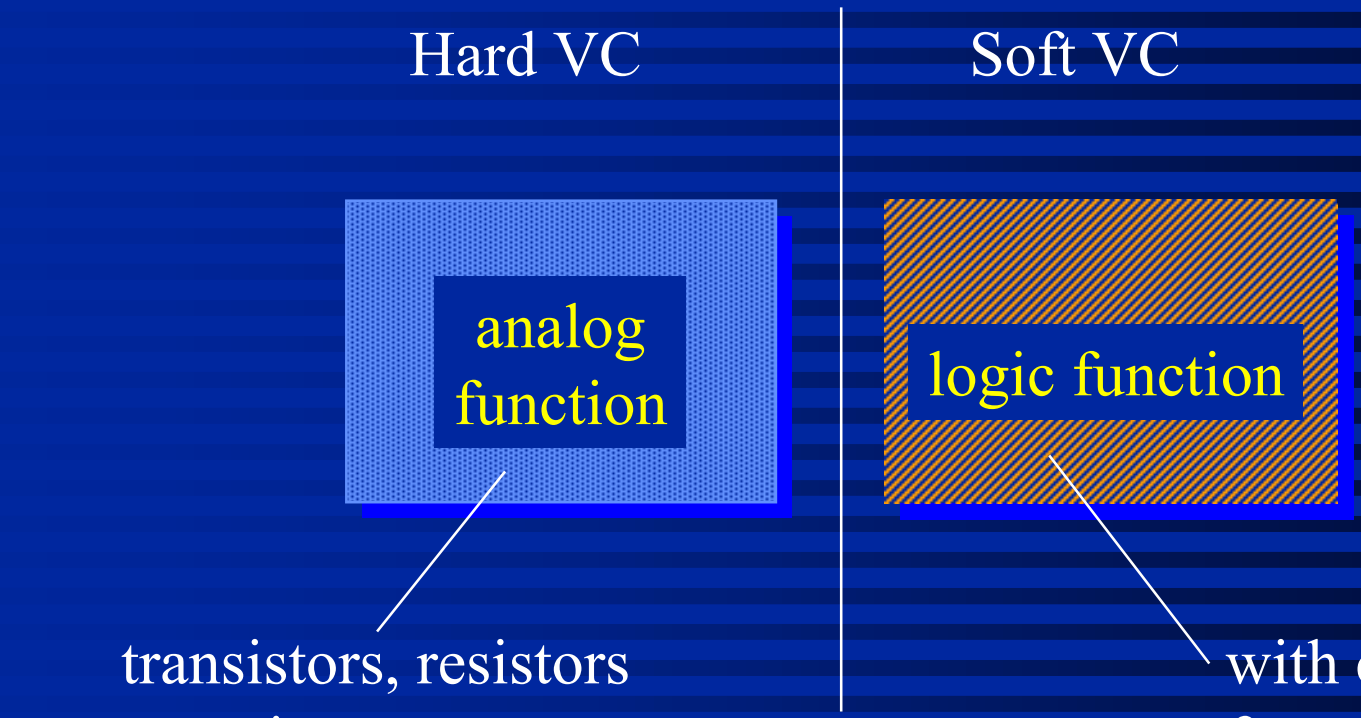
- Integration of Systems On Silicon needs:
  - interfaces with the analog external world
  - in the same advanced processes than complex digital functions
  - with the same constraints of time to market
- The answer is: Mixed Signal Virtual Components
- What kind of functions may be offered, what are the constraints



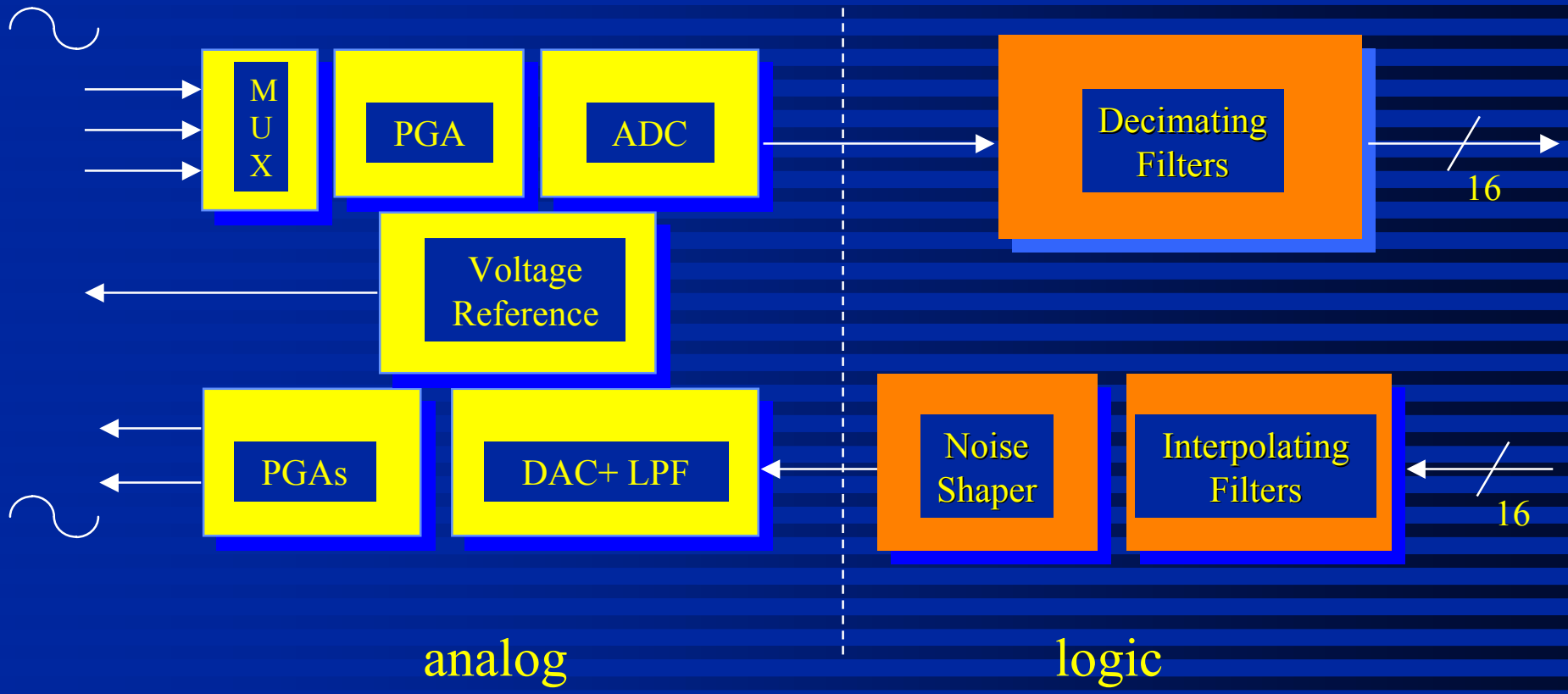
Dolphin Integration as a Mixed Signal VC Provider

- Created in 1985 as an independant Design Center
- 12 years of experience in logical and mixed signal designs
- Moved to VC Provider in 1995
- Customer references: TI, Motorola, NEC, SGS-Thomson µEM, AMS, ALCATEL, AEROSPATIALE…
- VSIA member since July 1997

What is a Mixed Signal VC?

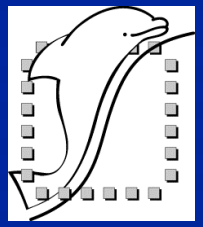


COLINE, Analog Front End for modems, fax, audio



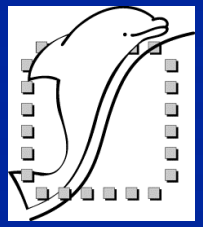
COLINE = Analog Front End for Fax, modems and audio

- Two existing optimized versions
  - one for 8 kHz sampling frequency
  - one for 9.6 kHz sampling frequency
- Easy derivation of existing versions for answering various needs: sampling frequencies, filtering characteristics



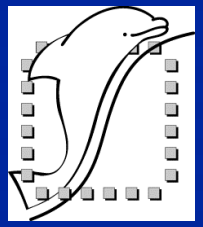
COLINE Characteristics (1)

- Main features
  - Single power supply 3.3 V ± 10%
  - Sampling frequency bandwith from 4 kHz up to 48 kHz, depending on main clock frequency
  - Filters compatible with G714 UIT recommendation
  - Power down mode, test modes offering different loops
  - Calibration mode in ADC for offset cancellation
- Performances
  - SNR and THD better than 80 dB
  - Low power consumption: typically 10 mW @ 8 kHz sampling frequency



COLINE Characteristics (2)

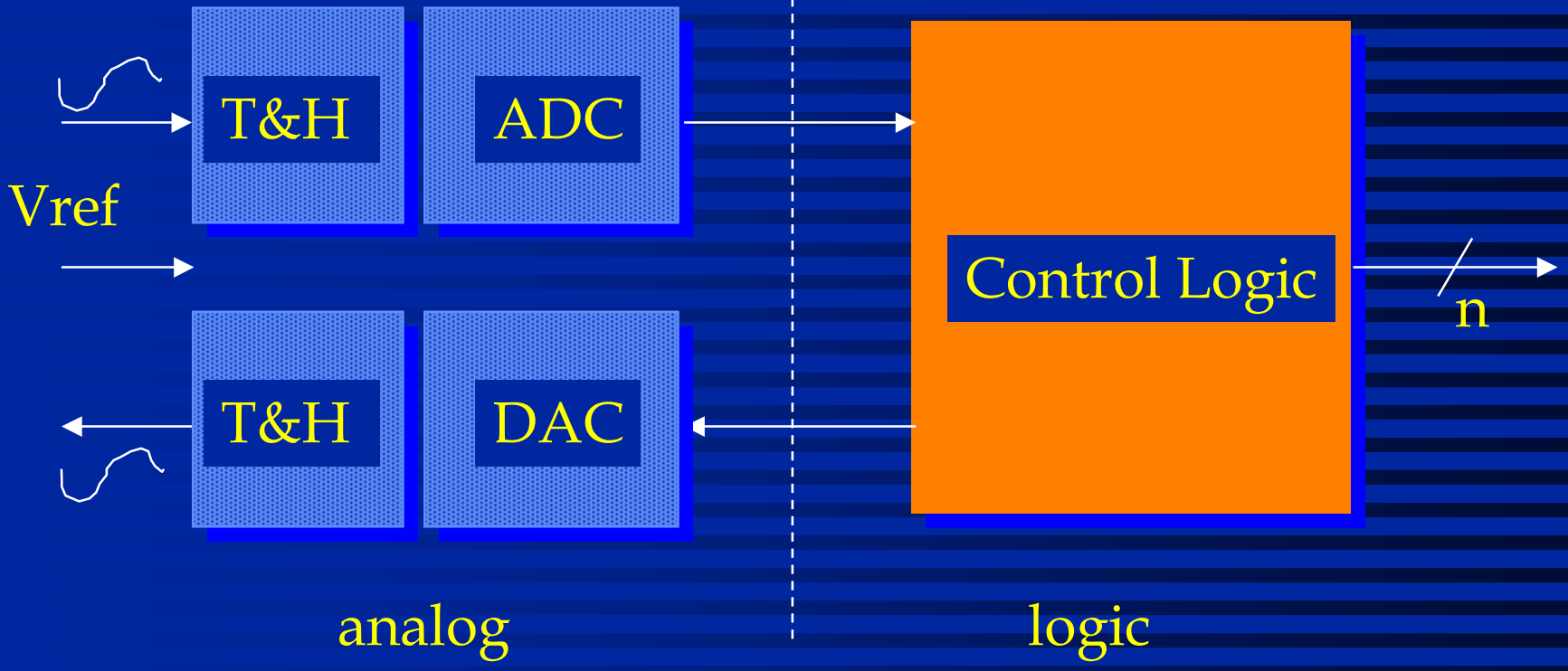
- 16 bit delta-sigma ADC and DAC
- Additional analog functions
  - Internal Voltage Reference
  - Analog input multiplexing
  - Analog programmable gain amplifiers on inputs: -6 dB up to 24 dB
  - Programmable gain attenuators on outputs: -30 dB up to 0 dB
- Retargetable toward any 3.3 V submicron CMOS process
  - Pure digital process for the ADC + DAC
  - With resistor and capacitor mask layers for the additional analog functions



COLINE Characteristics (3)

- Patented and silicon proven Operational Amplifier for switched capacitors filters: low noise, low power, low silicon area
- Silicon complexity
  - With a 0.35 µm CMOS process, three metal mask layers, one resistor and one capacitor mask layer
    - 0.25 mm^2 for the ADC + DAC
    - 2 mm^2 for the complete analog part
    - 14 000 gates for the digital part

LPCOD: Ultra low-power Codec



LPCOD, Ultra low power Codec

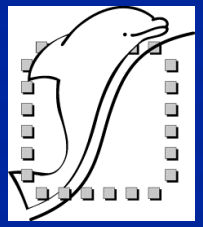
- Applications: dedidated for ultra low-power systems, e.g. hearing aids
- Algorithmic converters, patented realization
- Silicon proven

LPCOD Characteristics (1)

- Performances
  - 10 bits linearity, 14 bits dynamic range
  - Ultra Low power consumption: typically 130 µW for the Codec@ 8 kHz sampling frequency
  - Single power supply 3.3 V ± 10%, with possibilities down to 2.5 V
  - SNR and THD better than 58 dB
  - Sampling frequency from 4 kHz up to 16 kHz
  - Power down mode

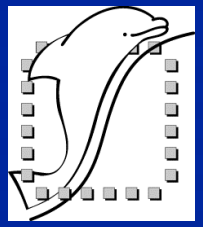
LPCOD Characteristics (2)

- Silicon complexity
  - With a 2 µm CMOS process, two level mask layers
    - 0.2 mm^2 for the complete analog part
    - 500 gates for the digital part
- Retargetable toward any CMOS process



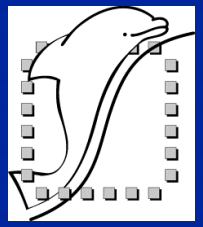
Mixed Signal V.C. Deliverables

- Logical part (soft VC)
  - VERILOG RTL synthesizable model and testbench
  - Functionnal test patterns
- Analog part (hard VC)
  - SPICE netlist
  - GDSII data base
  - Industrial test specification
  - Schematics (option)
  - Behavioral models (on request)
  - REPACK (on request)



Mixed Signal V.C. Deliverables

- Common deliverables for logical and analog parts
  - Specifications: description of the pins, the working modes, the electrical characteristics
  - User's guide for the integrator including
    - guide lines for connecting the analog and logical parts
    - guide lines for connecting the analog part to the pads
    - applications notes
    - various recommendations: power supplies, external connections…
  - Mixed signal behavioral model (on request)
  - Training / support / hot fax hot email/ yield support (on request)
- Our goal: compliance with VSIA specifications

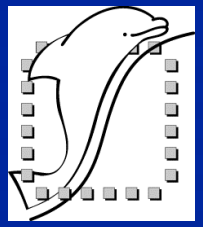


Design for Retargetability (1)

- Logical part
  - Verilog RTL models, easily synthesizable in any submicron process
  - No critical paths (maximum frequency = 6.4 MHz)
  - Synthesis scripts
  - Recommendations for clock and reset trees
- Analog part- The problem is how to retarget the hard VC in a new process and be sure that
  - The VC will work and respect the specifications
  - The retargeting design work will be done in a short time
  - No yield problems will appear during the production phase

Design for Retargetability (2)

- Dolphin answers for hard VC
  - Robust design rules including:
    - use of in-house generic device models with a wide variation range on key parameters (threshold, mobility, oxyde thickness)
    - use of robust schematics avoiding process dependant effects
    - rules for the layout and visual control for symetries, mismatch influences, power supplies lines, critical signals crossing, isolation between analog and digital

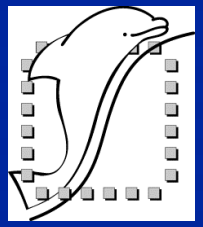


Design for Retargetability (3)

- Methodology for analog and mixed mode simulations
  - analog test bench containing the functionnal verifications test patterns and the worst cases for each sub-block of the VC
  - use of powerful tools like SHAKER (simulations iterations and data sheet extraction) and SMASH (mixed mode simulator) for improving the retargeting design work
- Analog test bench available as a commercial option: REPACK for REtargeting PACKage: allows an experimented analog designer to check the retargetability in another process

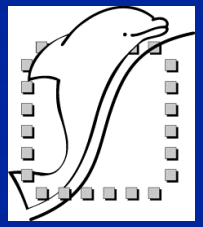
Design for Retargetability (4)

- Efficiency of the methodology
  - Using robust schematics does not mean poor performances and high silicon area: e.g. our patented OPA for switched capacitors offers an analog ²Σ AD modulator with 0.07 mm^2 in a 0.35 µm CMOS process!!
  - structure of the schematics are not changed through a retargeting, only slight dimensions of some devices have sometime to be made
  - layout retargeting work so is minimized but some rules have to be taken into accounts e.g. pad pitch constraints…



Quality and Time to Market

- First design of $2^{\square}$ converter required 2 years with two silicon runs
- Followed by 4 years of successful retargeting of high resolution converters in different CMOS processes
  - E.g. Stereo Audio Codec for Soundblaster boards
- Now, typically 3 to 4 months to retarget a complete Codec in another process with
  - High degree of confidence in the expected performances
  - High quality of the VC deliverables



CONCLUSIONS and TRENDS

- Mixed Signal Virtual Components are now a reality
- High Performances (resolution, ultra low power) are compatible with multi-process portability thanks to
  - Strict design methodology
  - Experience in analog design
  - Innovative patented solutions
- Next trends and planned mixed signal VC
  - High speed PLL (500 MHz)
  - 2nd generation of Audio Stereo Codec (1st generation available)
  - Flexible ADC for measurements applications