More work needed on mixed-signal VC front

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System-on-a-chip (SOC) designs involving mixed-signal virtual components (VCs) require integration with thousands of logic gates without noise interference. Meeting the challenges of this type of design, Dolphin Integration and NEC Electronics (Europe) recently created a Codec VC for audio and telecommunications applications.

The design successfully integrated A/D and D/A converters, programmable-gain functions and digital filters. Our effort resulted in some practical solutions to design problems, and demonstrated the deliverables needed for integrating mixed-signal VCs. Additionally, our experience led to some recommendations for the Virtual Socket Interface (VSI) Alliance "Analog/Mixed-Signal Virtual Socket Interface Extension" specifications.

A mixed-signal VC is formally defined as a macrocell integrating analog circuitry with logic functions managing finite-state signals, and implemented with gates. The Coline that we designed is typical of a complex mixed-signal VC. Basically, Coline is an analog front end for audio or telecommunications applications. Its compatibility with G714 UIT recommendations makes it suitable not only for fax and modern communications, but also for voice Codecs.

Coline contains a Codec (A/D + D/A) with ancillary analog functions. The analog parc of the A/D contains a multiplexer that allows the user to choose between three analog inputs and a programmable-gain amplifier (PGA), and a delta-sigma modulator that includes a patented operational amplifier.

The analog part of the D/A contains a switched-capacitor low-pass filter with two output drivers designed for low-impedance loads. The internal voltage reference makes the VC complete and independent while eliminating the need for additional external analog components. The logic part of the design contains the decimating filters associated with delta-sigma modulator, interpolai-11g filters and delta-sigma noise shaper
for the D/A converter.

The VC works with a single 3.3-V power supply, and typically presents 10 mW for an 8 kHz sampling frequency. It offers signal-over-noise ratio and distortion of 83 dB. Sampling frequencies up to 50 kHz are available by a simple change of main clock frequency. The device measures 2.5mm^2 and was biult on a O.35-micron, three-layer metal CMOS process, with one capacitor layer and one resistor layer. Its density is about 13,000 gates.

When the VC integrator acquires a macrocell, the major deliverables are specifications that include details on pins, working modes, timings and electrical characteristics; a GDSII database together with a SPICE net-list for the analog part of the VC; an RTL model together with a test bench, functional test vectors and synthesis scripts for the logic part of the VC; a user's guide; and a test methodology.

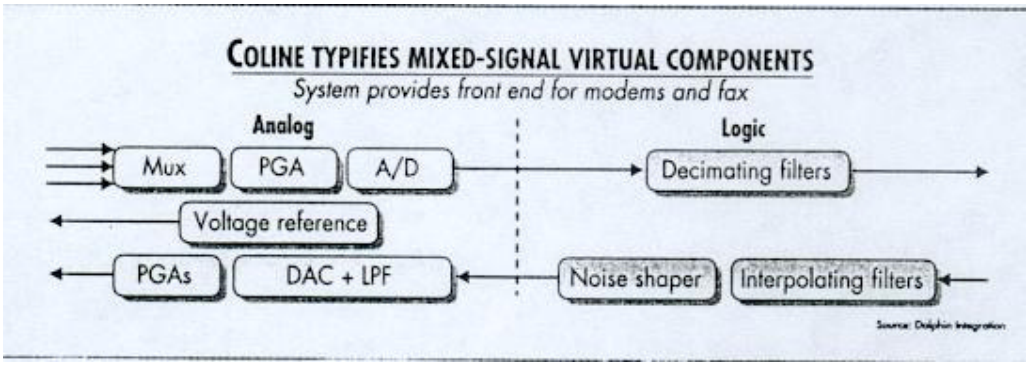
For complex mixed-signal VCs, the VC provider usually participates in the test and characterization of the first chip. This leads to more deliverables, including a validation plan containing hardware and software descriptions for characterization, measurements, and a characterization board. For Coline, the characterization board included the circuit to test analog-signal conditioning and a field-programmable gate array (FPGA) for interfacing with the measurement tools.

Pure-logic VCs are available as soft, firm, and hard as specified by VSI. For Coline, the logic part is described as a soft VC; its RTL model is delivered together with a test bench and synthesis scripts. The necessary high performance of the analog part of a mixed-signal VC like Coline relies on the schematics and layout. This implies that the analog part be delivered in a hardware (GDSII) format. However, retargeting must be performed before delivery. In general, the VC provider and the integrator must agree on the targeted process. Depending on the VC and its performances, it maybe retargeted in a pure-logic CMOS process, although occasionally some analog process options like a resistor layer and a capacitor layer are needed.

This is often the case when programmable-gain amplifiers or attenuators are used. In any case, the retargeting tasks include re-simulation of schematics with target-process models and parameters, and retargeting of the layout to make it compatible with target-process layout rules. Retargeting work for a complex VC like Coline typically takes three months at Dolphin, far less than what it takes to develop the same function from scratch. In addition, Dolphin's portable design rules work with a design flow of intensive simulation and automatic extraction of electrical characteristics.

First-pass silicon is facilitated by mixed-signal simulations used with Dolphin's Smash product during the development and retargeting stages.

NEC's goal was to put Coline in an ASIC library. This required Dolphin Integration to adapt the VC to the specific design flow and led to several important constraints. First, the VC had to be connected to a test bus used at the VC integrator for industrial test of the library macro cells. This required the development of Verilog-HDL blocks to interface the VC and the test bus. Second, it was necessary to edit a special user's guide to include the test-bus interface. Third, a new testbench and test vectors had to be generated. The original test bench and test vectors had been provided for testing the VC itself, but not the VC plus the test-bus interface.



The second constraint resulted from specific design rules for devices connected to the pads. These were a mix of electrical rules, ESD protection rules, and layout rules for output transistors. This required Dolphin to re-design and re-layout the output stages for analog output amplifiers. The third constraint concerned the layout of the analog part. Some I/O pitch was required for packaging reasons, so the original layout had to be modified. Such basic cells as operacional amplifiers, delta-sigma modulator and voltage reference were not altered, but the respective placement and rooting of these basic cells were modified to respect the new I/O constraints without degrading performances of the overall function.

From a general point of view, more support was required than anticipated. NEC found some difficulties when it attempted to use the VC in configurations not imagined by Dolphin. These included special usage of stand-by mode and changing sampling frequencies on fhe fly. Both led to changes of application notes and data exchanges within the documentation. For the VC provider, the time required to meet these demands was relatively small compared with the time spent on initial overall development.

Prior to implementing Coline in its library, NEC had to perform certain tasks. First, Dolphin had to run logic synthesis, check fault coverage using the test vectors supplied, place-and-route the logic part, and run the back-annotated simulation. After each step, NEC had to check against the test bench and vectors to ensure that the new reference model gave the same simulation

results as the golden reference RTL model. In addition, the logic and analog parts had to be interconnected to realize a hard block.

It appeared that the first release of the user's guide was not detailed enough on this point. It was then decided to provide a more detailed description of the interconnection, including text, block diagram and files. Additional requirements became evident during the project, mainly for complementary documentation in various fields for ASIC designers. A comparison with the "Analog/Mixed-Signal Extension" specifications issued by the VSI Alliance to its members was conducted after the design was completed. It was concluded that VSI specifications provide an excellent guideline.

The experience of Dolphin Integration and NEC Electronics allowed both partners to suggest improvements for the Analog/Mixed-Signal specifications. These lmprovements were presented during the VSI Alliance World Wide Member Meeting, held on March 25 in Santa Clara, Calif. They included enhancement of the description of the "prototype evaluation method" byadding a design flow for complex mixed-signal VCs; the delivery of a characteization board, specification and user's guide for such a board; and a validation plan for testing the VC inserted in a first circuit.

VCs like Coline have an internal voltage reference. This voltage reference is built with parasitic bipolar transistors, often poorly characterized in the targeted process. Thus, the user's guide must show ways of toning this reference voltage. Descriptions including text, block diagram and files for the interconnection of analog and logical blocks at the highest level are mandatory.

Both partners now contend that mixed-signal Virtual Components associated with professional support and documentation methodology allow design reuse and enable aggressive time-to-market. However, intense work has to be invested by everyone involved in extending usage of mixed-signal VCs. This will include virtual testing for automating the link between simulations and the industrial test, as well as agreeing on different levels of accuracy for behavioral analog simulations.