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The Awaited Standards for safe integration of mixed signal Virtual Components into logic systems

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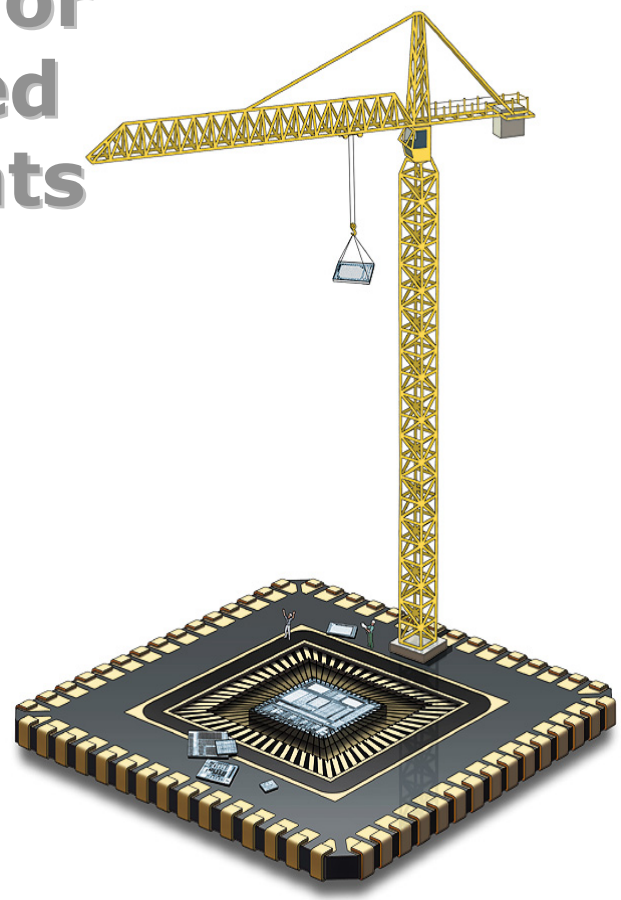

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Outline

- Company brief
- To mix or not to mix analog with logic?
  - The « Non-Silicon-Proven » syndrome
  - What analog expertise does the use of mixed signal Components (ViC) require?
  - Virtual Disturbances from logic <-> analog modeling
  - Requirements for a quality metric and standards
- Conclusions

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The Tripod of our offering

Symbolic gift from one of our Chinese partners

- A strong synergetic potential between:
  - **Silicon intellectual Property Products**
    - Embedded memories
    - Mixed signal: ADC, DAC, PLL
    - 8b, 16b microcontrollers
  - **EDA Solutions**
    - "Missing EDA Links" for hierarchical mixed signal design
      - SMASH: mixed signal simulator
      - SUCCESS: cosimulation HW/SW
      - …
  - **Dolphin Delegation Services**
    - Four professions in growing demand for design in Microelectronics
- Since 1985, now 160 skilled personnel
- On EuroNext OTC stock-market
- 10 M€ sales turnover

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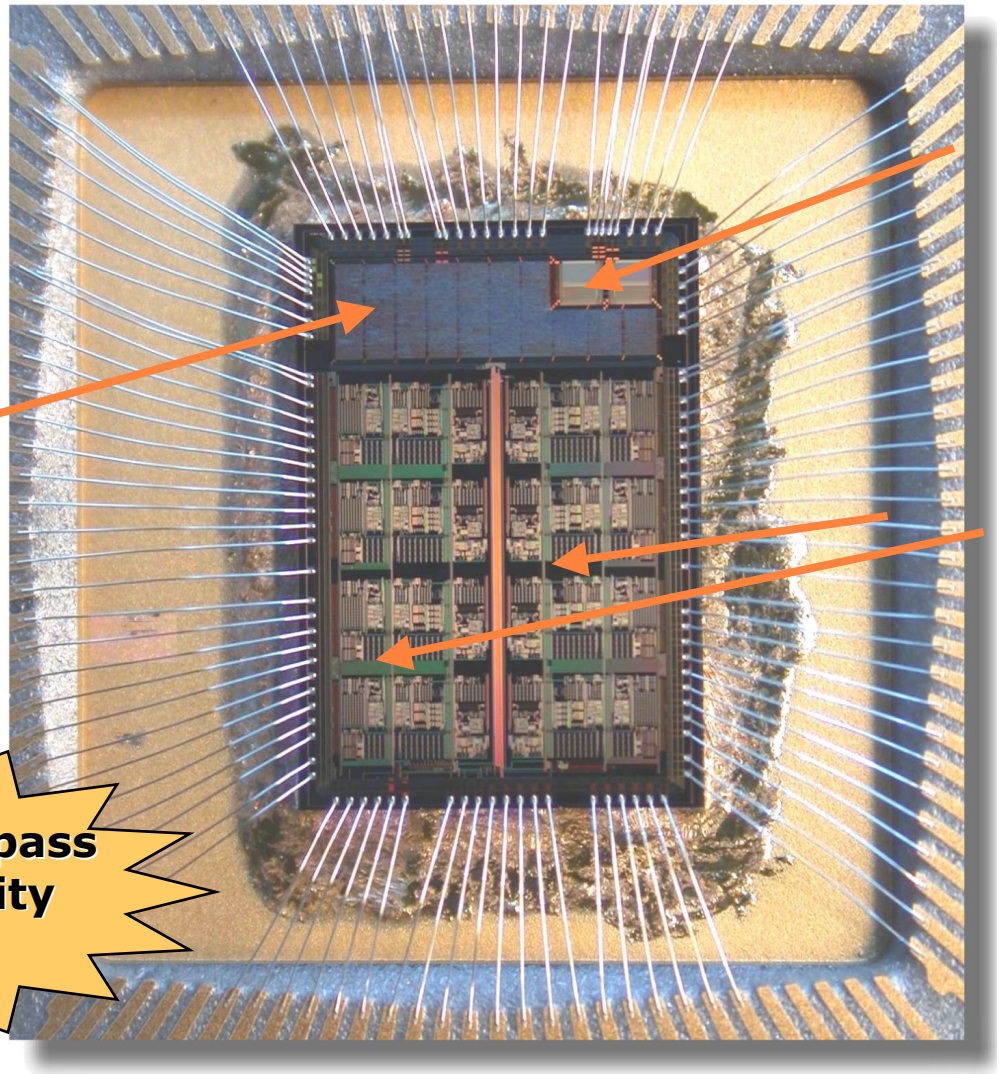
Our mixed signal expertise



Logic

Memories

High resolution Analog/Digital Converters

Right-on-first pass
High Reliability
High Yield

Onboard the A380

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To mix or not to mix? -1

- The « Non Silicon Proven » syndrome…
- …or why an « ostrich policy » has to be replaced by:
  - A quality standard
  - The « Virtual Fab » procedure

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Specifics of analog design

1. **Automatic top-down analog synthesis is doomed:**
   - Electrical competency needed
2. **Analog design is a bottom-up process**
3. **Large number of foundries for analog with process variants**
4. **Huge number of specification variants**
5. **High sensitivity of analog to process features**
6. **Lack of experienced analogdesigners in the world**
7. **There is a long way from analog design IP to an analog ViC!**

More than 90% of needs for mixed signal ViCs are not available "as is"

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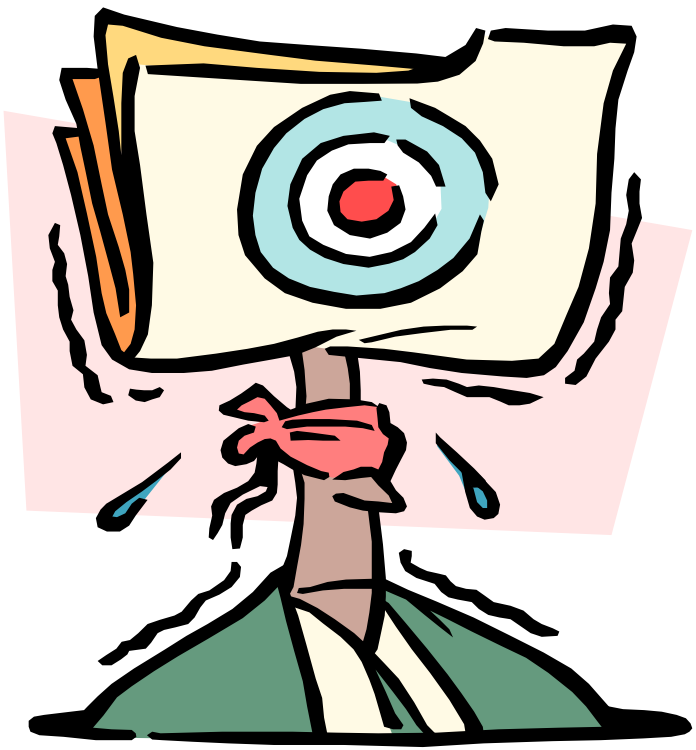
Coping with the NSP syndrome « Not-Silicon-Proven »

- **« Silicon Proven » samples alone do not prove anything!**
  - **Risks due to poor Design Yield during production are not covered, even by simulations of traditional "corners"**
  - **Risks due to the mix of the ViC with other functions is not covered**
  - **M$ may hang there!!**



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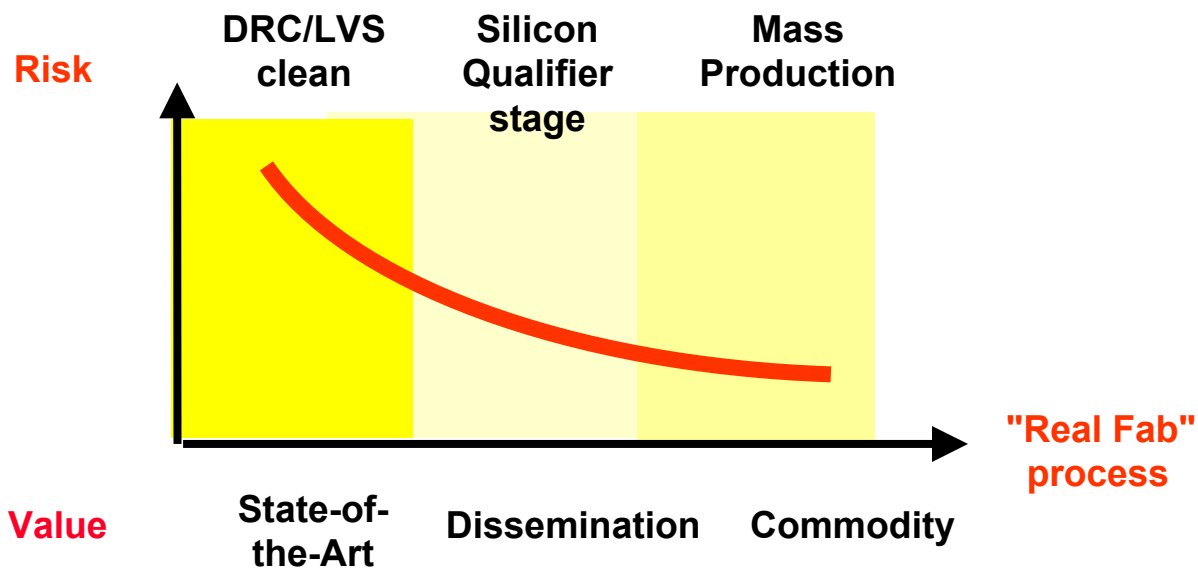
Risk-Taking for New Product TTM

What is the problem?

Risk minimization between failing a design…
… and missing a time-window



New product TTM is not compatible with a double-qualification cycle: at ViC level and at SoC level!

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Risk-Taking for New Product TTM

- The wrong solution:
  - The Not-Silicon-Proven syndrome
- Waiting for 100% certainty of design security is the sure killer of product competitiveness:
  - Either missing a schedule, or by-passing a crucial innovation

RISK = VALUE

QUALITY = EXHAUSTIVITY and RELIABILITY OF TESTBENCH + DESIGN YIELD assessment

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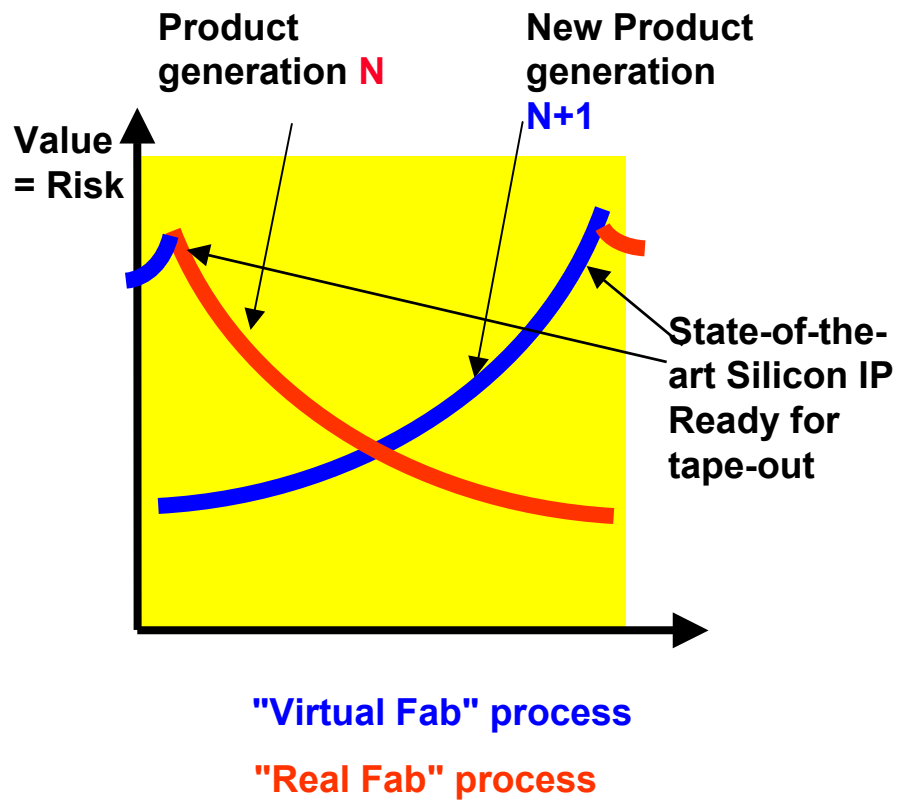
The "Virtual Fab" procedure to make the mix feasible

- The single solution: « some » silicon qualifications wisely meshed with:
  - Robust design processes
  - Design yield assessment during simulation
  - Extended quality procedures
  - "Stress inside" for noise resilience sensitivity
  - … and driven by teams with experience!!
  - Qualify your IP partner and its design methodology, millions of $ are at stake!



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To mix or not to mix? - 2

- Is embedding mixed signal ViC in a SoC reserved to mixed-signal experts only?
- Or how quality standards and dedicated support can make it possible for logic designers as well!

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Analog ViC to be used by logic designers

Requires complete set of deliverables and support, including:

- FTDM: Functional Timing Digital Model (per VSIA)
  - To be used with pure logic simulators
- Virtual Sockets for hierarchical DRC and LVS
  - But framework independent
- Specifications for industrial testability
- On-request support for test and characterization

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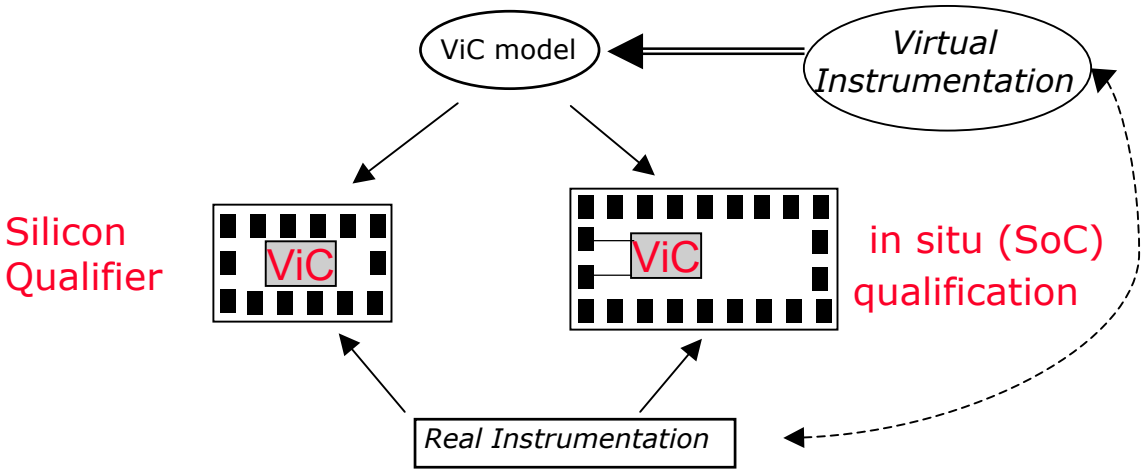
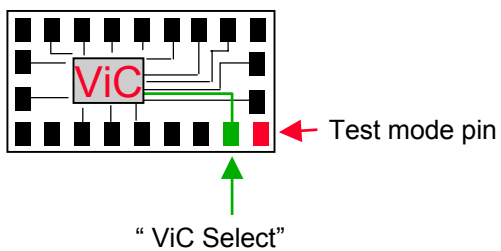
SoC design for industrial testability





SoC in test mode
for Virtual Qualification of ViC

- Capability of isolating the ViC for its test and characterization at SoC level:
- Enables optimization of industrial test programs
- Accelerates diagnostic of functionality, performance and yield
- Allows to measure the Influence of the rest of the SoC on ViC performances

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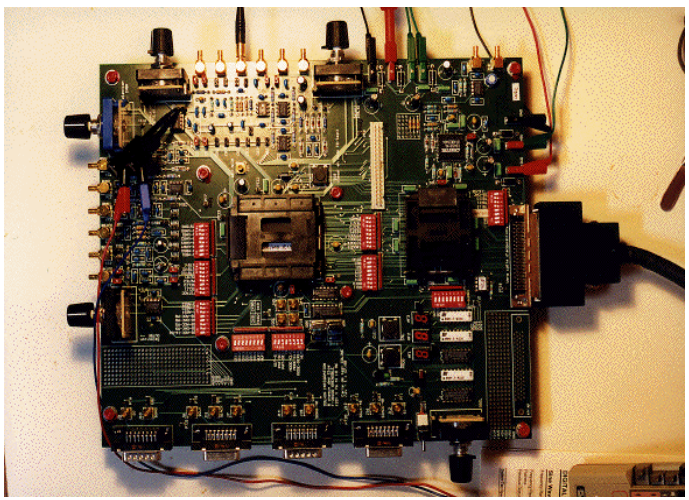
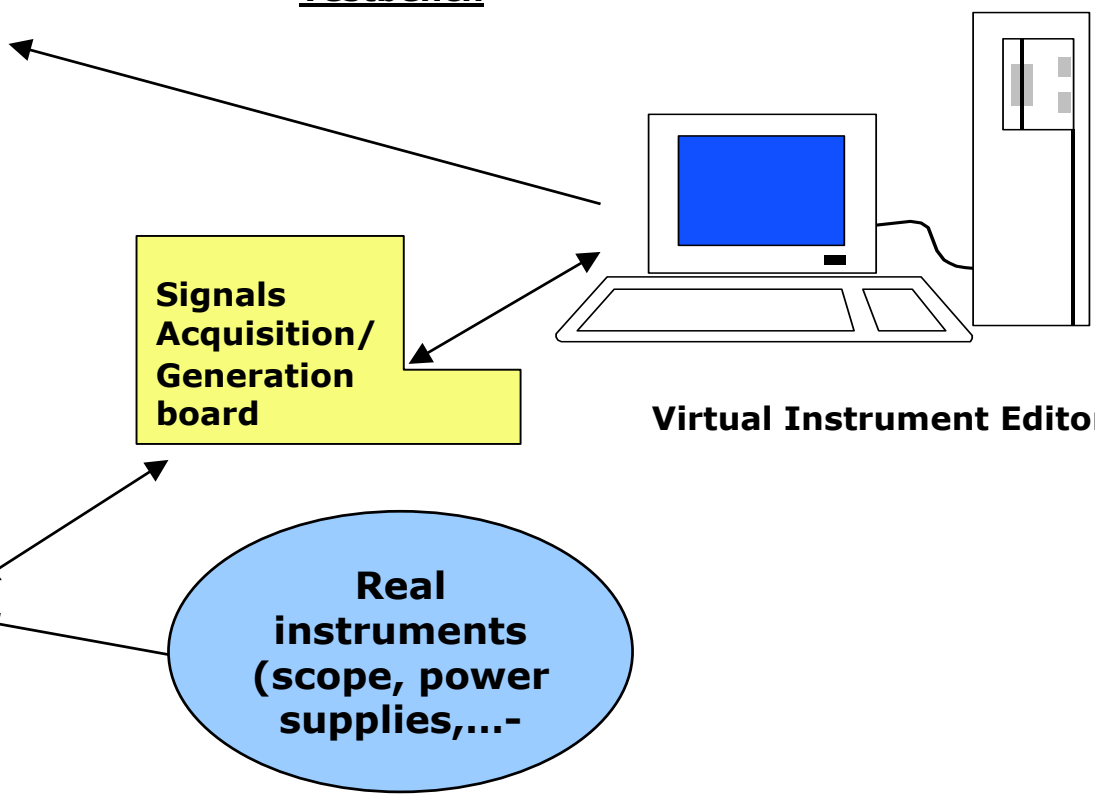
Service for ViC Test and Characterization

Real test at prototyping level:

Testbench

QuickTime™ et un décompresseur GIF sont requis pour visualiser cette image.





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To mix or not to mix? -3

What about the on-SoC disturbance hassle between analog and logic?

- How to face the issue dodged by PCB designers for lack of simulation skills

- Or how to move progressively from **Black Magic** to **Mixed Signal mastery** by relying methodically on novel standards

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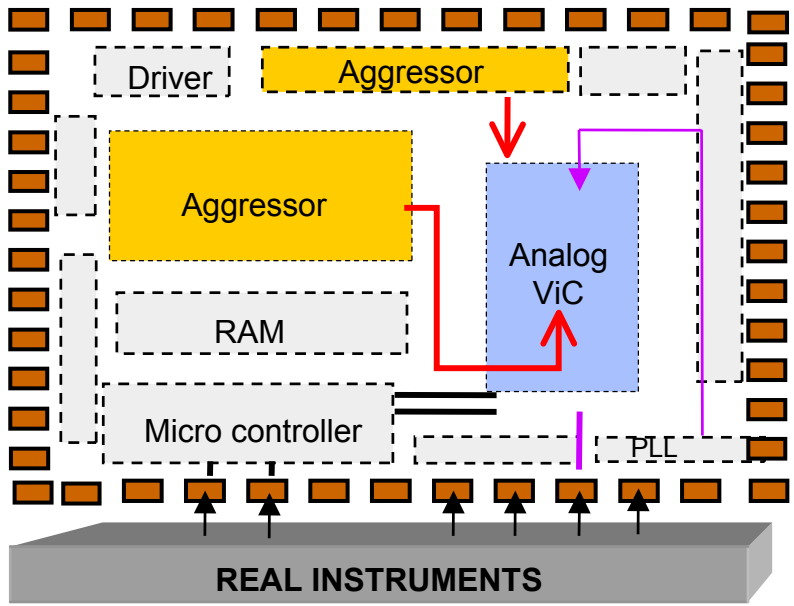
SoC Logic disturbs the ViC

- Tough issue: Assessing the various disturbances generated by the blocks of the SoC itself, that directly impact the level of performance of the Virtual Component.
- Sensitivity : SNR, THD, Jitter…
- IDRT: Injected Disturbances Rejection Threshold, given as the noise threshold above which the related ViC is not compliant to specifications anymore.



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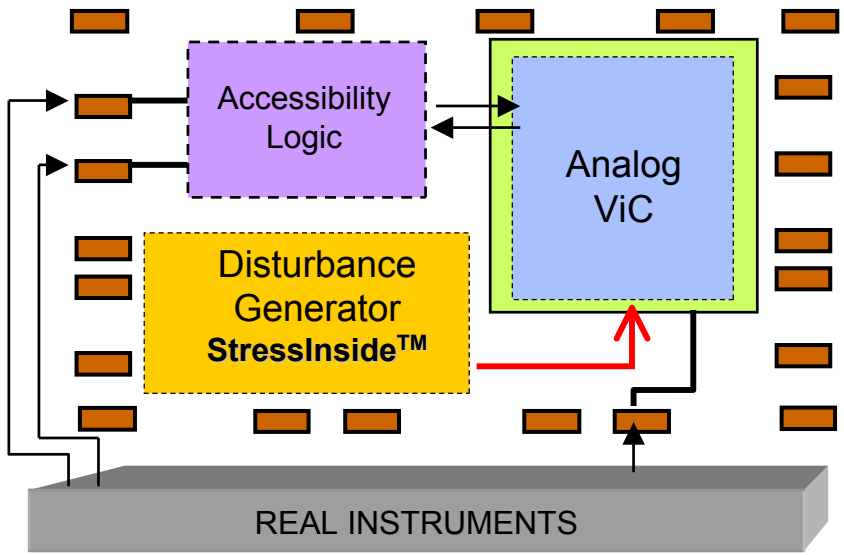
StressInside™: a Disturbance Generator

For a successful SoC integration:

- A testchip for A&MS ViCs sensitive to SNR, THD or Jitter is pointless.
- What counts is the capability to access the preservation of performances, whatever the environment due to a specific SoC.
- The latest DOLPHIN innovation: Programmable StressInside™, to emulate the "normal" disturbances expected from a SoC: random spurts, periodic spikes, asynchronous events...

Real Silicon Qualifier (Testchip with StressInside™)



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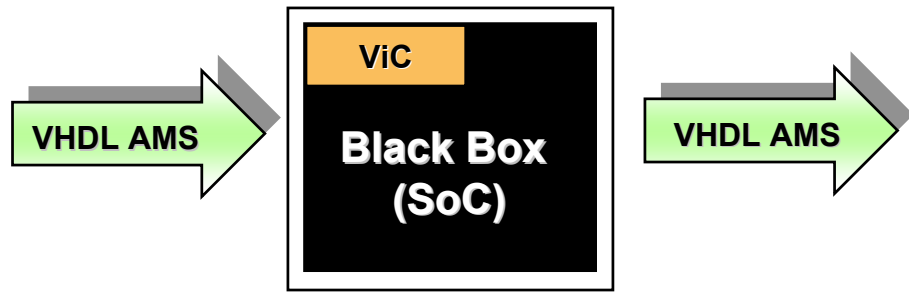
Modeling of SoC disturbances

Worth of a testchip for A&MS ViCs sensitive to SNR, THD or Jitter: validate the adequacy of defense mechanisms of the ViC against the Noise and Stress injection of a specific SoC.

- Joint Modeling Method:
  - The SoC architect must provide a model of all the SoC disturbances generation capabilities
  - The ViC designer must supply the modeling technique for Stress injection, and hypothesis of their injection port
  - The ViC designer must supply the model of his « Chinese Wall », as diverse « Defence Mechanisms » that must be sufficient against the specific Disturbance Invasion from each SoC.
- => Demonstrate the IDRT is adequate for the aggression profile of each specific SoC



Analog modeling dedicated to the evaluation of the SoC disturbances:
The SoC seen by the ViC as an analog Black Box!

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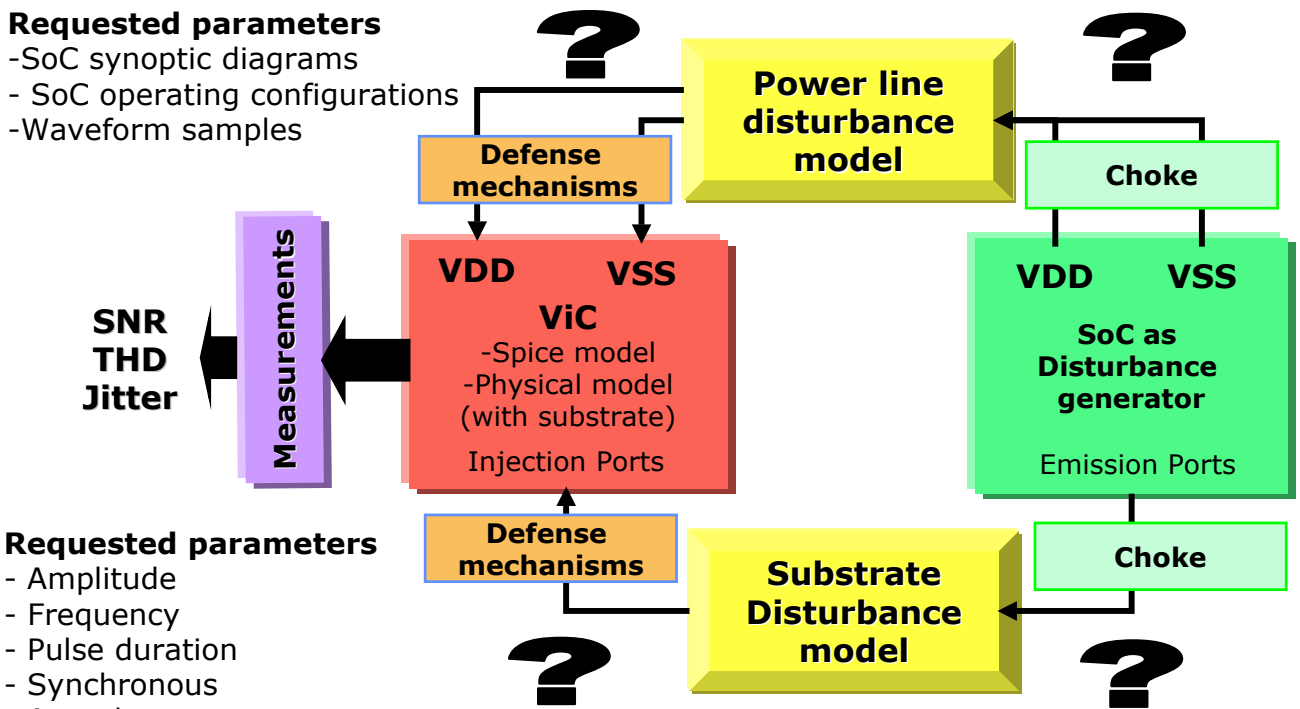
Synthesis of the joint method for modeling SoC disturbances on ViC

The ultimate SoC Integration mastery provides the reciprocal solution to disturbance Reception, as a "choke" on disturbance Emission, where Self-Control of the SoC takes into account the IDRT sensitivity of the ViC.



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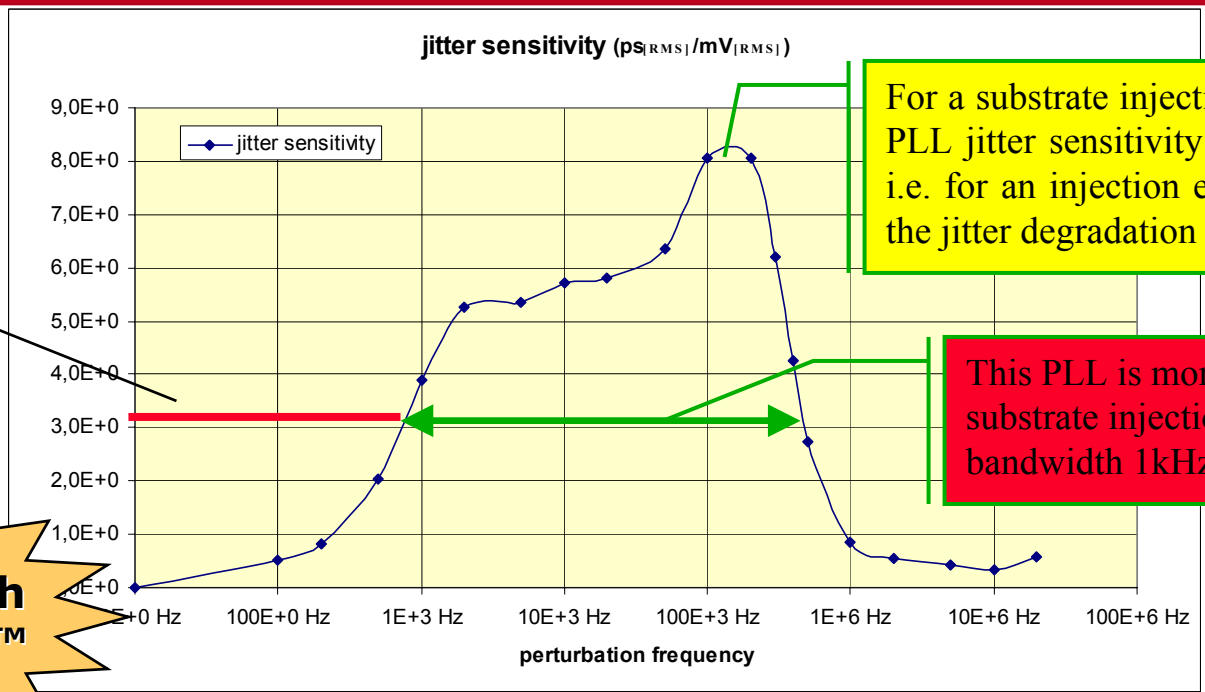
Example of the sensitivity of a PLL jitter to injected noise

Example of IDRT for the PLL



For a substrate injection at 100kHz, the PLL jitter sensitivity is $8ps_{RMS}/mV_{RMS}$, i.e. for an injection equal to $20mV_{RMS}$, the jitter degradation is $160ps_{RMS}$

This PLL is more sensitive to substrate injection in the bandwidth 1kHz to 500kHz

Measured with StressInside™

- The jitter sensitivity function gives the degradation of the ViC characteristics due to the substrate noise injection

- Allows to define recommendations and constraints to embed the ViC in a SoC
- Allows to compute the final characteristic of the ViC embedded in a SoC

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To mix or not to mix - 4 Awaited Standards

- Our contribution (available on request) to QIP metric promoted by FSA and VSIA for a better risk and maturity assessment:
  - Add qualification questionnaires on design methodology and management of critical issues: noise, jitter, local dispersions, design yield
  - Clarification for a ViC: what is really new, what has been migrated from another process…
  - Qualification of the IP provider experience

- New methods for evaluation of disturbances effects from SoC -> mixed signal ViC
  - IDRT definition
  - Noise emulator
  - Modeling method

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Conclusions

- Mixed signal Virtual Components can be used by logic designers
- The choice of a qualified IP supplier with a global offering (product + services) is of paramount importance for the success of a mixed signal SoC from the specification to the mass production
- For innovative mixed signal ViCs and SoCs, the complete « virtual fab » method is more reliable than a mere « silicon proven » approach.
- Critical aspects (noise) of integration of mixed signal ViCs can be addressed by a methodological approach
- New standards are required to improve the use of mixed signal ViC by SoC integrators
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