



Analog & Mixed Signal IC Debug: A high precision ADC application

Introduction

Increasing pressure on production costs and, more generally, time to market, have impacted all levels of IC design. In this context, one of the major challenges is to avoid silicon failure or yield loss. Indeed, a widely accepted statistic today is that almost half of all designs fail at first silicon. Failure costs are obviously due to new mask generations, and additional engineering time, but also to the potential miss of a large part of the market window for a product. Therefore, first-pass silicon success and high design yield has become a fundamental requirement for IC designs, and is, quite naturally, driving an increasing need for integrated circuit verification and debugging solutions.

Debugging is a methodical process of finding and reducing the number of defects. Thus, any software solution will never replace the designer's know-how. Nevertheless, to assist designers in this cumbersome task, the goal of the debugging solutions is to identify defects before silicon runs. In this article, we report how the use of appropriate CAD solutions helps us design a high-resolution ADC good in first silicon pass.

sensADC-16.02 - ADC for low frequency sensors

Measurement applications in low frequency domain imply stringent requirements in terms of noise management for high-resolution conversion. **sensADC-16.02** (a Dolphin Integration product) is a complete configuration of a $\Delta\Sigma$ ADC core and peripherals performing high gain amplification while guaranteeing low noise signal processing for the best noise-free resolution. It digitizes into 16 bit words the low level signals generated by a transducer, thanks to a programmable gain amplifier, an analog sigma-delta modulator and a digital low-pass filter.

The aim of this article is not to study the circuit itself but to describe some classic and critical issues of a complex design. Indeed, three aspects are discussed (Figure 1):

1. Circuit characteristics impacted by process dispersion,
2. Circuit characteristics sensitive to local dispersion,
3. Circuit characteristics impacted by high impedance nets.

Design Yield – Process Dispersion

When designing at SPICE (block) level in current nanometer technological processes, a particular attention should be paid to process variations which are the cause of device mismatch and dispersion. For example, circuit sensitivity to non-uniformities of a fabrication process is a key issue for many analog signal-processing circuits (such as sigma-delta modulators). The accuracy and performance of their functions relies on the matching properties of certain devices.

Monte Carlo analysis is the classic way to help assess design robustness, identify alternatives that can reduce design failures, and help ensure satisfactory performance of the design in different operating modes. The first lack of this approach is its inability to pinpoint which components are directly responsible for a given failure. To address this issue, it is mandatory to go beyond Monte Carlo, in order to investigate precisely the runs that have unexpected results.

Imbalance Locate is a unique, SMASH™ patented, post Monte Carlo based analysis. The aim is to discriminate wrong runs with the Monte Carlo analysis, and to reproduce these runs in different modes [1] in order to identify faulty devices. The procedure requires four simple steps:

1. Run the Monte Carlo analysis to evaluate performances in different operating conditions (in our case, we pay attention to settling time in a pre-amplifier),
2. Identify defected runs which have caused errors or which have caused degradations of circuit characteristics,
3. Run an Imbalance Locate analysis on the previous defected runs to identify faulty devices that are responsible for the errors or degradations,
4. Once the guilty devices have been found, you can modify their characteristics until the run matches the specifications.

Applying this functionality to the ADC pre-amplifier block, we evaluated a sequence of settling time measurements to locate which devices may be responsible of failures. These settling time values are critical to ensure good performance of the amplifier, and should be stable through process variation. Imbalance Locate has allowed us to identify which set of transistors has caused the errors cases. Without any direct designer know-how, Imbalance Locate analysis helps us to identify the 7 transistors over among 450 transistors of the first stage preamplifier that are responsible for dispersion on settling time performance.

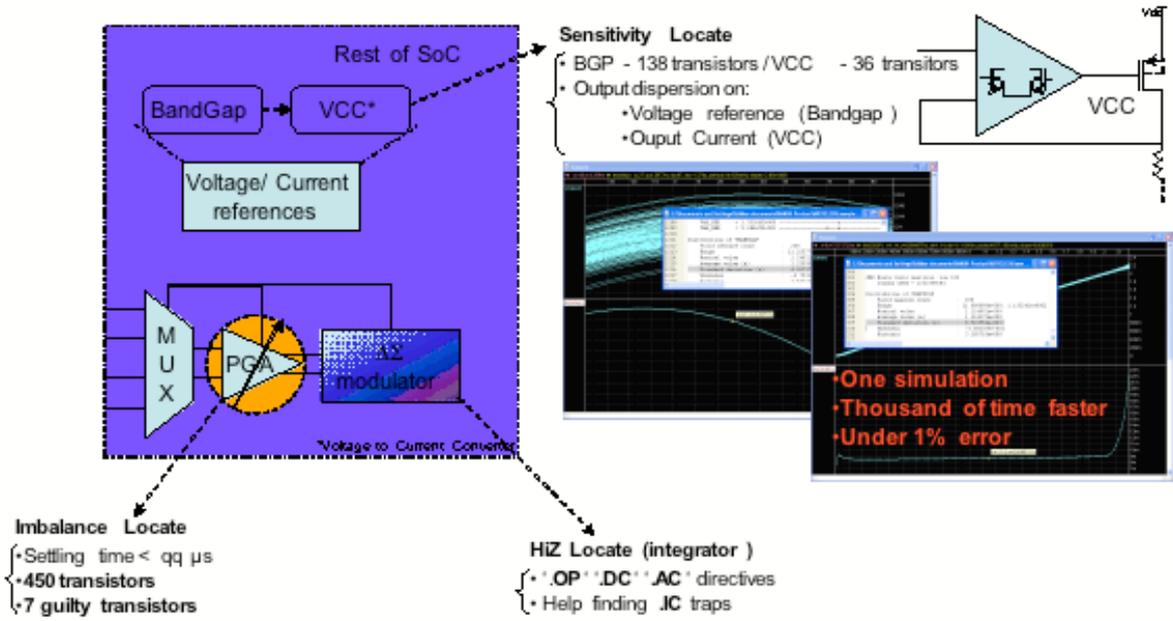


Figure 1: CAD solution for IC design and debug

Design Yield – Local Dispersion

The other well-known lack of Monte Carlo analysis is the very long simulation time required to perform a thorough statistical analysis with sufficient individual simulation runs. In the case of local dispersion, these numerous simulations can be replaced in SMASH™ by a single Sensitivity Locate analysis. Indeed, to determine offsets or drift on critical nodes, local dispersion can be simulated for the operating point, DC and small signal analyses. Moreover, this approach provides the contribution of each device to the total dispersion, allowing discrimination of the elements at the origin of the dispersion. This local dispersion sensitivity analysis has been applied successfully to determine dispersion on the ADC bandgap and VCC (Voltage to Current Converter), see Figure 1.

Dispersion of each circuit characteristic has been found with less than one percent error, in a simulation time thousands of times faster than classic Monte Carlo [2].

Hi-Z Nets

To complete the set of yield debug features, Hi-Z net or floating net detection is of utmost importance. While useful when used appropriately, e.g. in amplifiers for large voltage gains without large current consumption, in tri-state outputs for data busses, in standard cell library cells... unintentional high impedance nets are a frequent cause of non-working circuits, e.g. due to major leakage resulting from short-circuits to ground... while practically undetectable with functional simulations. In most complex designs, detection of Hi-Z nets and characterization of net impedances has become a deterministic issue to avoid silicon failure. In order to detect or characterize high impedance nets, we have to consider both analog and digital problems. In digital cases, a Hi-Z wire can generate power consumption and is very sensitive to coupling effects. In analog designs, high impedance nets have high thermal noise and are prone to pick up. They are also often difficult to probe as the impedance of a scope can load down the node.

Hi-Z detection must allow locating both structural (schematic) as well as electrical high impedance nets. This functionality has been used on a sigma-delta integrator block.

A classical trap in analog design is to fix some voltages with .IC directives, in order to obtain an operating point, forgetting that these initial conditions will disappear on silicon. Thus, it is quite necessary to be warned of the existence of Hi-Z nets at the operating point step (for example) to remind the designer of danger induced by “artificial states”. Typically, the presence of high impedance nets hidden by “.IC” directives has been detected on the sigma-delta integrator (Switched Capacitor based).

Conclusion

The growing complexity of designs has placed designers in the intractable situation where they need a lot of know-how and guess work to check their IC designs. To help designers face the design challenges of complex, mixed-signal and multi level designs, the Dolphin Integration mixed-signal multi-language single kernel simulator SMASH™ offers a complete design environment with a suitable set of features to debug analog and mixed-signal designs before the first silicon run.

The robustness of the design of a complex IC, such as our sensADC-16.02, has been increased thanks to the following features:

- Thorough diagnostic of circuit bugs causing yield losses, beyond Monte Carlo with Imbalance Locate for precise pinpointing of devices at the origin of design yield losses due to process dispersion.
- Unique capabilities for fast sensitivity to on-chip dispersion diagnostic, without the burden of lengthy Monte Carlo analysis, to find the elements that are sensitive to dispersion and contribute the most to the total dispersion.

- Efficient Hi-Z net detection and impedance evaluation, including floating net detection at operating point and during transient analysis, with tracing of resistive and capacitive impedance of SPICE nets for all analyses (system and block level).

Considering that 50% of designers' time, on any circuit, is spent at debugging, or even proving the absence of bugs, this article has described three analog debug features that allow to identify critical nets and devices in order to increase design robustness and reduce probability of silicon respin. These unique capabilities make SMASH™ a crucial add-on to any analog or mixed-signal design flow.

REFERENCES:

[1] Tutorial Imbalance Locate, <http://www.dolphin-integration.com>

[2] Tutorial Sensitivity to dispersion, <http://www.dolphin-integration.com>

Frédéric POULLET,
Senior Application Engineer