An Analog Front-End for Remote Sensor applications with High Input Common-Mode Rejection including a 16bit ΣΔ ADC in 0.35µm 3.3V CMOS process.

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Abstract: ***Data acquisition through remote sensors can be exposed to very high electrical noise sources because sensor wiring act like antennas for noise. Aircrafts are particularly exposed to EMI, RFI radiations and IxR ground loops.***
The chip 'OctAD-16' has been designed for digitizing various DC and AC signals coming from onboard sensors with reduced loss of accuracy even with 150V and several 100MHz electrical aggressions.
A standard 3.3V CMOS process without high voltage option has been chosen to insure a long production life of the chip.
In this paper we describe the design solutions we have used to cope with such stringent requirements.

Index terms: ADC, CMOS, common-mode rejection, sensor, drive-by-wire, fly-by-wire, sigma-delta, EMI, RFI, EMC, ground loop, lightning, BCI (Bulk Current Injection)

1. Introduction

Continuous improvements in data acquisition systems, computer and sensor technologies lead to a generalization of "drive by wire" controls in vehicles. In such applications, drive by wire replaces complex mechanisms found in traditional steering, brake, clutch, throttle controls by lighter electrical wires.
But it is not always possible to digitize analog signals close to the sensor, particularly when it is located in hostile environments that cannot be supported by data-acquisition electronics. This is particularly true for aircraft industry where sensors face freezing temperatures of flight surfaces in high cruising atmosphere or automotive with hot temperature near engines or brake discs. As a consequence, the sensors must be remote to the data acquisition equipment, requiring long cable runs in areas were high levels of electromagnetic interferences may be encountered. This enable to locate the electronic into more friendly temperature and mechanical environment.
Interferences can take the form of:
-Electro-Magnetic Interference (EMI) emitted by computers, power motors, power lines, lightning, cosmic radiation, nuclear strike. Aircrafts are particularly exposed to lightning EMI (150V spike).
-Radio Frequency Interference (RFI) generated by radios and transmitters, cellular telephones, radar and electronic navigation systems (several 100MHz AC signal).
-IxR ground loops: the current that flows in the system ground resistance generates voltage errors between grounds. Corrosion, humidity or loosened nuts can degrade ground connection quality after years of operation.

2. Main Circuit Requirements

-Input signal maximal differential amplitude is ± 10V. It can be pseudo differential, fully differential or floating. Useful input bandwidth is DC to 6kHz.
-Maximal common mode interferences amplitude is ± 150V.
-Common mode frequencies range from DC to several 100MHz. The most severe frequencies are above 1MHz.

In this context, the circuit must:
-Extract, filter and digitize the useful signal into 16kHz, 16-bit words
-Suppress common mode AC noise
-Meet the specified input impedances.
-The input analog sampling rate is 1024kHz
-Signal/noise ratio > 85dB
-Out-of-band differential attenuation > 85dB
-Out-of-band common mode attenuation > 85dB
-Eight identical analog input channels

This paper emphasizes the common mode rejection input stage, which is one of the most critical function of OctAD-16 circuit. The design challenge is to digitize with minimal error the useful differential signal riding on high amplitude -up to 150V-, and high frequency -several 100MHz- common mode aggressions. According to our knowledge, no published paper describes some realization with such common mode requirements.

3. Circuit Description

A fully differential implementation is chosen for its immunity to noise pickup. The input stage must amplify and filter the differential useful signals and must suppress the common mode signals. Good instrumentation amplifiers have typical Common Mode Rejection (CMR) ratings of 90dB up to 100kHz. In our case, CMR must be better than 85dB up to several 100MHz. With such high frequency common mode aggressions, a classical instrumentation amplifier is no longer valid, because the common mode signal is suppressed with the same circuitry that carries the useful low frequency signal. In other words, parasitic and useful signals share the same analog path and it is very

difficult for an amplifier to pass accurately low frequency signal if it is overloaded with high amplitude/high frequency common mode signal.

3.1. Straightforward approach

First of all, we decide to use some kind of resistive divider to attenuate the high common mode perturbations in order to fit the ADC input common mode range. This allows to keep the high voltage constraints outside the chip.

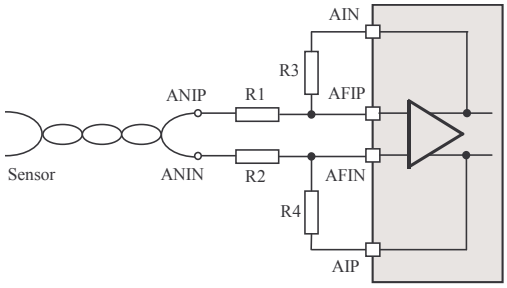


Fig. 1. Fully differential amplifier with limited input common mode range

The straightforward approach uses a fully differential amplifier with an output common mode biased near VDD/2=1.5V.
The weakness of this solution is the low input common mode range which is limited by amplifier inputs common mode AFIP, AFIN and external resistor values. If we consider a 0.25 differential voltage gain between (ANIP, ANIN) and (AIP, AIN) and a 3V power supply, the maximum common mode range of the sensor wiring is ±7.5V. This low common mode range is not acceptable.

3.2. First possible implementation

On Fig. 2, external resistors R1 to R4 perform the necessary differential voltage attenuation for keeping useful differential signals into the ADC input range. In this implementation, the common mode is removed by a feedback loop embedding two matched current sources I1, I2 and a differential amplifier.

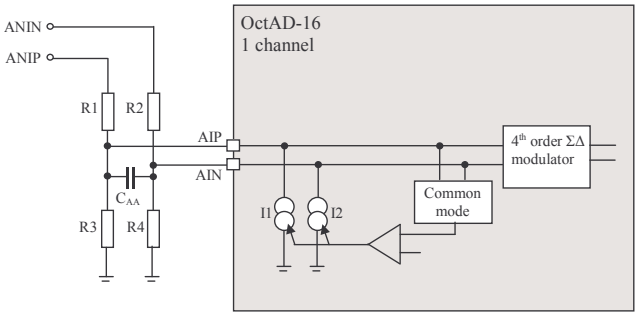


Fig. 2. First implementation with common mode rejection stage.

With a voltage gain equal to 0.25 (external resistor ratio), a ±10V input signal between ANIP, ANIN will lead to ±2.5V at the modulator input AIP, AIN.
With such a schematic, chip designer can set independently the differential gain and the common mode rejection. This is easier to handle for the final user since he does not have to care about common mode for resistor value calculations.
The small signal equivalent circuit shown on Fig. 3 helps to visualize that the circuit has two distinct input impedances. This explains why common mode signal is rejected while differential is left unchanged.

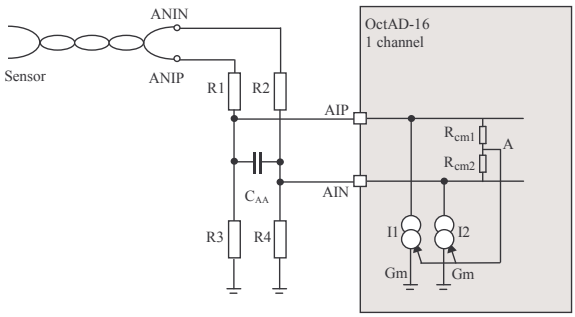


Fig. 3. Simplified common mode rejection small signal schematic.

Looking into the circuit in common mode, the input impedance is proportional to $1/G_m$, G_m being the voltage controlled current sources transconductance. As a consequence, common mode input impedance is low.
Looking into the circuit in differential mode, the voltage potential at node A is constant. Current sources I1 and I2 are constant, their impedance is ideally high. The impedance of the common mode "resistors" Rcm1, Rcm2 can also be made high. As a consequence, differential input impedance is high.

To work properly, the common mode circuitry must have a frequency bandwidth higher than the common mode aggressions maximum frequency, i.e. several 100MHz. This will guarantee the correct biasing of nodes AIP, AIN for all kind of perturbations. If the bandwidth is too low, high frequency perturbations may push AIP, AIN inputs outside ADC input common mode range.
The maximum available I1, I2 currents is sized to keep the inputs correctly biased during transient spikes due to lightning or IxR ground drop.

The resistors matching is critical. Otherwise, input common mode is transformed into differential signal at AIP, AIN nodes and is added to useful signal. This leads to an error since the distinction between real differential signal and common mode residues cannot be made anymore after they are added together.
With 0.1% accuracy resistors, the common mode attenuation is close to –60dB at the modulator input while signal attenuation is –12dB. So, if we consider that useful signal and common mode have the same amplitude, the signal/noise ratio will be only 48dB.
Therefore, the 85dB SNR target requirement is not fulfilled.

Since a simple resistive bridge is not efficient enough to reject high frequency common mode perturbations, C_{AA} capacitor has been added (fig. 3).
This external capacitor C_{AA} presents a twofold effect: it performs anti-aliasing filtering and suppresses high frequency common mode signals that are incompletely removed by the two resistive dividers due to their mismatch. This means that resistor matching is only relevant below RC_{AA} cut-off frequency. Beyond cut-off frequency, the remaining common mode component is further attenuated through low pass filtering. The RC_{AA} cut-off frequency is set to 20kHz to leave useful differential signal unfiltered. This first order low pass filter attenuates by 20dB/decade leading

to –34dB at 1MHz. This component will be aliased back into the useful bandwidth noise floor by the sampling modulator. With the initial –60dB attenuation this results in –94dB at 1MHz while signal attenuation is –12dB. The signal/noise ratio is then 82dB.
Therefore, the 85dB SNR requirement is still not fulfilled.

3.3. Final implementation

It appears that a second order active filter must be used to meet the specifications. If high frequency perturbations are applied to such filters an accuracy degradation arises as amplifier open loop gain degrades with increasing frequency. As previously explained, amplifiers do not like high frequency perturbations while trying to pass accurately low frequency signal.
For that reason, we have chosen a "Rauch" active filter that uses a pure passive RC cell at its inputs in order to maintain filtering efficiency beyond amplifier bandwidth (Fig. 4).

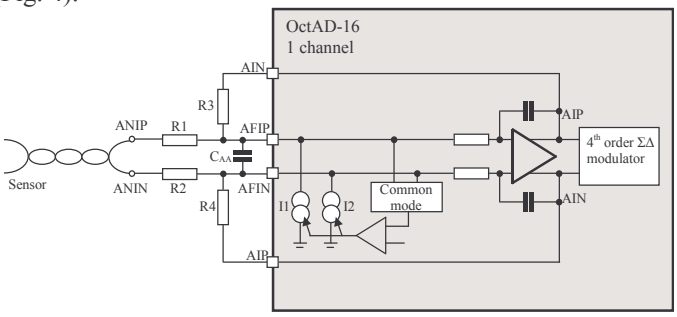


Fig. 4. Final architecture embeds passive linear RC filter and common mode rejection loop. Only 'clean' useful signal pass through differential amplifier

The four external resistors are now used in a feedback configuration to adapt the ±10V input signal to the ±2.5V ADC input range. C_{AA} capacitor performs an efficient low-pass filter input cell before the active filter part.

Now, the differential amplifier can work in a more friendly environment, only low frequency differential signal remains: The out–of–bandwidth differential signals are removed externally by passive RC and the common mode aggressions are removed by the common mode rejection loop.
Resistor values R1 to R4 are chosen for differential gain, thermal noise and input impedance.

This 2nd order filter rejects common mode components by 100dB at 1MHz before there are aliased back into the useful bandwidth by the sampling modulator. Signal attenuation is -12dB, the signal/noise ratio is then 88dB.
Therefore, the 85dB SNR requirement is now fulfilled.

4. I1, I2 Matched current sources MOS design

The current sources outputs are labeled AFIP, AFIN on simplified schematic Fig. 5. Their output common mode voltage is sensed with two PMOS differential pairs MP1 to MP4 and compared to circuit analog ground VMC (1.5V). The error current is sunk or sourced to both outputs through current mirrors. This arrangement for differential pairs is well known for its reduced linear input range. But as these pairs are connected between nodes AFIP, AFIN (fig. 4) it is usable in our application for the following reasons:

-For low frequency signal (DC to 20kHz), the voltage difference between AFIP, AFIN is small because of the amplifier high open loop gain.

-For medium frequency signal (20kHz to 10MHz), this voltage difference remains small due to C_{AA} capacitor lower impedance when increasing frequency.

-For high frequency signal (10MHz to several 100MHz), the schematic can reduced to its high frequency path only (fig. 6)

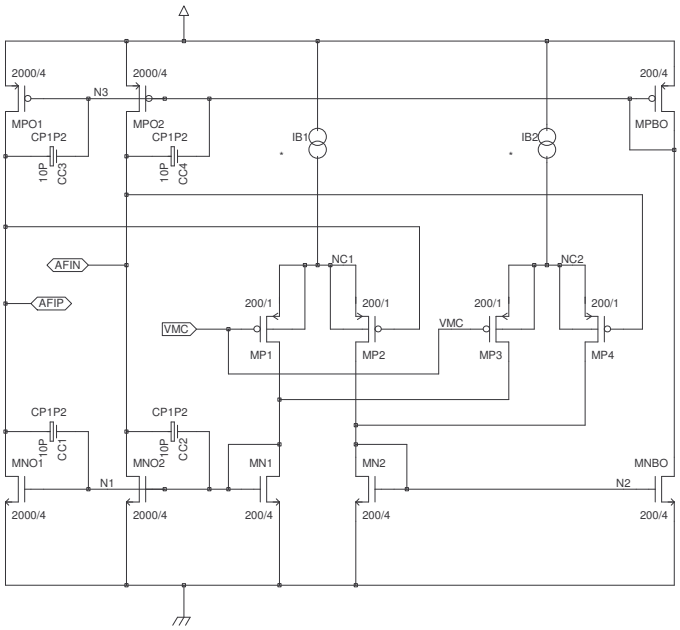


Fig. 5. DC to HF Common mode matched current sources

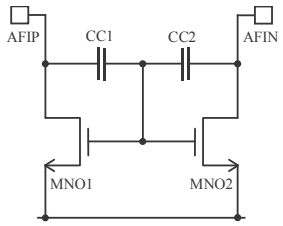


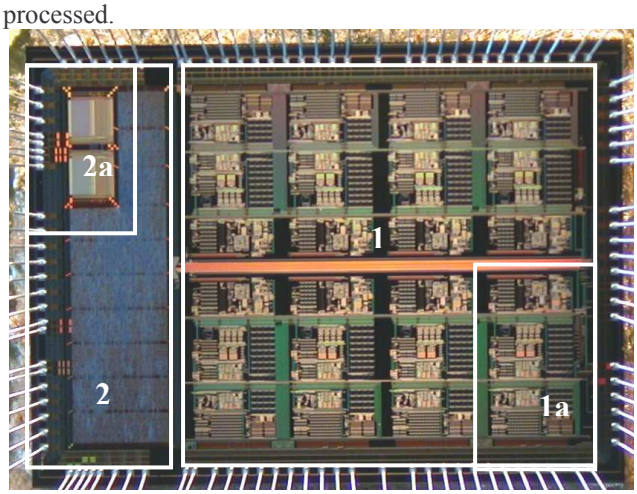
Fig. 6. High frequency equivalent schematic. The overall feedback loop is removed due to its frequency cut-off.

On Fig. 6, the input stage has been ignored because we can consider that the input path corresponding to differential pairs MP1-MP4 is cut-off around 10MHz. The remaining components are those included in the AC high frequency path: output TMOS, MNO1, MNO2, MPO1, MPO2 and feedback capacitors CC1 to CC4 (Fig. 5). The simplified schematic on fig. 6 shows only the NMOS part, PMOS part being symmetric.
CC1 and CC2 purpose is to bypass input stages at several 100MHz frequency. High frequency common mode on AFIP, AFIN is rejected by low $1/G_m$ impedance while differential signal is left unchanged. This explains why the common mode rejection loop is efficient up to the highest frequency aggressions.

Prototype die photo

OctAD-16 chip has been processed in a 0.35µm CMOS 3.3V with analog capacitor option. It embeds an analog (1) and a digital part (2). The analog part embeds 8 identical channels

(1a). Each channel integrates a common mode rejection loop, a low pass filter input stage and a 4th order ΣΔ modulator.
Digital embeds a two-stage decimating low-pass filter, 8 high-pass filters and 2 SRAMs (2a). Output datas are displayed on a tri-state serial interface. This allows to cascade several circuits if more than 8 channels need to be processed.



5. Silicon measurements

The signal connection to the circuit inputs can use pseudo-differential, fully-differential, floating or grounded wiring.

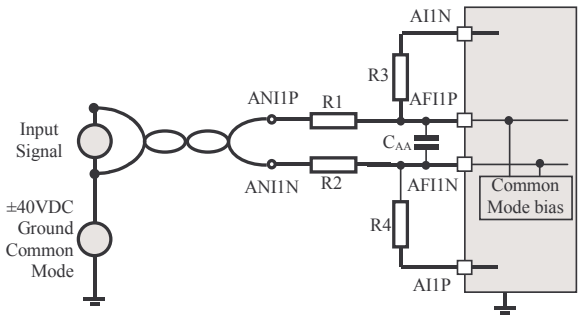


Fig. 7: Test fixture for SNR and THD measurements with grounded wiring. Input signal: 10V peak sine wave @ 400Hz superposed to a ±40V DC signal. Bandwidth 0Hz to 6kHz.

The following table summarizes some performances of the data conversion with the presence of DC common mode signal. The test configuration for THD and SNR measurements with a ±40V DC ground difference between sensor and acquisition circuit is shown on Fig. 7.

PERFORMANCES MEASUREMENTS Power Supply Voltage 3.0V to 3.6V. R1=R2=100kΩ±0.1% R3=R4=25kΩ±0.1% Master Clock frequency Fmclk=4096kHz Digital output sampling frequency Fs=16kHz.		
PARAMETER	**Test result**	**UNITS**
SNR (Fig. 7)	> 88	dB
THD (Fig. 7)	< -85	dB
Interchannel isolation	> 103	dB
Power Supply Current	< 90	mA

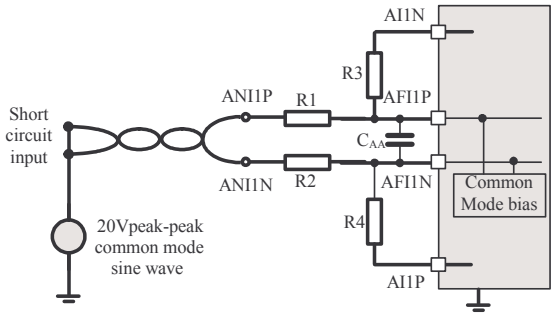


Fig. 8: Test fixture for Common Mode Rejection measuremets

The graph of Fig. 11 shows the circuit Common Mode Rejection (thick line) compared with two commercial amplifiers (thin lines). It shows clearly the higher common mode performances of OctAD-16 above 100kHz, where EMI and RFI aggressions are the most severe.
The small dip noticeable near 300kHz is due to the chopper circuitry.
This common mode response is often difficult to find in standard commercial products especially at high frequencies.

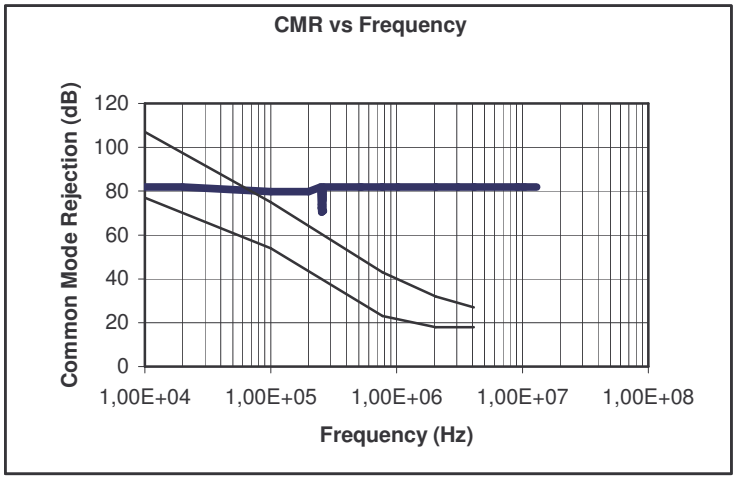


Fig. 11. Measured Common Mode Rejection (thick line) compared with commercial amplifiers (thin lines)

5. Conclusion

Problems arising when interfacing remote analog sensors dictate the use of input stages that remove 150V, several 100MHz common mode parasitic signals. As a consequence, common mode rejection input stage is one of the most critical function of the OctAD-16 circuit. Published papers or standard circuits datasheet do not describe such common mode requirements.
This circuit prevents the data corruption due to EMI, RFI and lightning effects encountered by in-flight aircrafts.
The OctAD-16 chip has been developed in partnership/customer relationship with Airbus France.

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