A GSM RECEIVER BASE BAND IN 0.25µ, 1.8V FULLY DEPLETED SOI INCLUDING A 4th ORDER SERIAL ΣΔ A/D CONVERTER.

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Abstract

SOI technology is very promising for digital low voltage low power devices, but radio integration requires also the base band analog and the RF circuits to be realised in the same technology for a single chip radio. In the analog circuits we learn to live with the kink effect and in the RF we benefit from the low drain&source to bulk capacitance. In this paper we report the obstacles encountered in the base band analog design for a GSM receiver and the 4th order serial sigma delta architecture.

Index terms-SOI, GSM, filters, switched capacitor, sigma delta converter.

1. Introduction

Bulk CMOS transistors are difficult to modelize near the threshold voltage of the device. This region of biasing is the moderate inversion regime and represents the "junction" between week and strong inversion.

With SOI the problem is even more present with the added difficulty of floating body voltage. This effect leads to an increased drain current for a drain voltage exceeding roughly ≈1V.

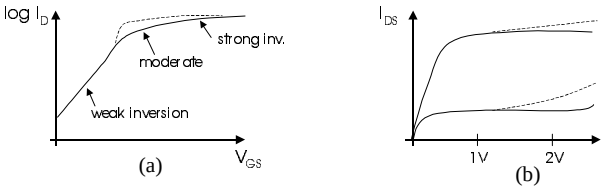

Fig. 1. Typical SOI output characteristics (dashed lines) compared to Bulk CMOS.

Fig. 1 shows output current Id vs gate (a) and drain (b) voltage. In (a) plain line shows the drain current for a low drain voltage smaller than ≈1V and dashed line shows the drain current for a drain voltage exceeding ≈1V. In (b), a bulk CMOS characteristic is represented with plain lines and SOI MOS with dashed line.

This current increase is called kink effect and is caused by impact ionization when a high electrical field appears near the drain diffusion. Holes generated by this effect increase body potential and therefore modify the threshold voltage. Only NMOS are affected.

Another important point is that this increased drain current is frequency dependent : if gate or drain voltage are swept fast enough (10MHz) during the measurement, the output current will not show this kink in its characteristic and will look like indicated with plain line.

For fully-depleted devices, it occurs only just above threshold voltage and at high drain voltage.

2. Circuit description

The receiver base band circuitry which has been implemented is composed by an input continuous time filter, a continuous time Low Pass Filter followed by a 4th order Sigma Delta modulator ADC and a decimator by 8 digital filter.

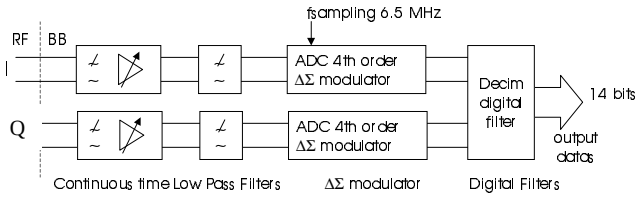

Fig. 2. I & Q base band block schematic. The goal is to filter and amplify the 100 kHz GSM band and remove out-of-band signals.

The two I and Q channels are identical and multiplexed within the digital decimation filter. The main function is to reject out-of-band signals and to amplify the GSM 100kHz band. The Signal/Noise ratio for the whole chain has to be greater than 78dB. This is a real design challenge for this 1.6V-2.0V SOI 0.25µm process.

2.1. Design procedure

At process level designers can reduce kink with a reduction of silicon film thickness. Another way is to use a specific process design which connect the body potential. Such design also increases the capacitance but induces another limitation : maximum channel width must be around 10µm to have an efficient body bias. But this leads to a great number of fingers in case of a wide channel. This is not possible in analog circuit because we need big W/L ratio for matching, low V_{DSSAT} and low flicker noise. Then we used a thin fully depleted silicon film with floating body.

At schematic level we used such structures that are kink tolerant by applying following guidelines to avoid or minimize kink :

-Make NMOS work under low V_{DS} voltage.
-Use cascode and « shield transistors » to isolate the

drain from the « high voltage output V_{DS} > ≈1V.

-Make tolerant schematics to process variations and modelization inaccuracies.

-Use local feedback in order to linearize the response.

In this SOI process, the design procedure was to inspect all NMOS : devices operating under small drain voltage were left unchanged but high drain voltage devices were to be modified (Fig. 3) in order to reduce their operating drain voltage. Current increases dramatically for a simple current mirror were the reference NMOS operate at low V_{DS} and the other NMOS at high VDS. In this configuration, the current ratio can be as high as 10 for identical matched devices.

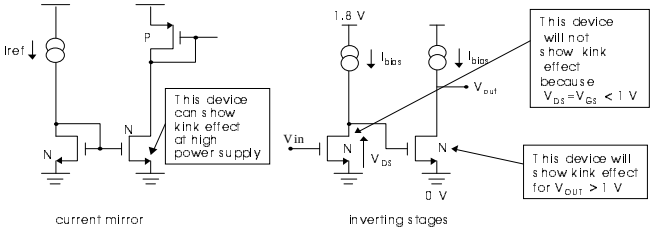

Fig. 3. Current mirror and inverting stage kink sensibility

We used two means for drain voltage reduction :

a) Linear cascode device

This is the "classical" cascode device inserted in serial with the signal device. In this arrangement, both devices must remain saturated. Accuracy is guaranteed when used within open loop structures like master bias current mirrors (Fig. 4).

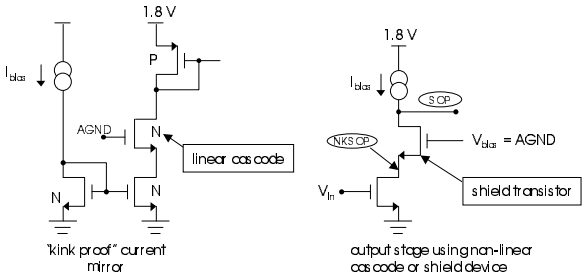

Fig. 4 . Current mirror and inverting stage modification.

b) Non-linear cascode or shield device

Cascode devices are known for reduced output voltage swing and impossible to use in a 1.8V±10% power supply design.

In our case we allow the cascode to enter in the linear or unsaturated region. This is not a problem as we don't use it for gain enhancement but only for isolating high output voltages from the transistor's drain. For small output voltages the cascode is pushed down into its triode region (unsaturated) thus the isolation action disappears but the drain voltage is small enough to avoid kink. This non-linear action does not degrade performances if it is embedded within a feedback loop. For example, this shield device has been used in all amplifiers output stages of the base band design.

The simulation curves show (Fig.5) the reduced drain swing on the sensitive signal device. We can see that drain voltage V(NKSOP) does not exceed 0.4V. This will assure that kink will be avoided.

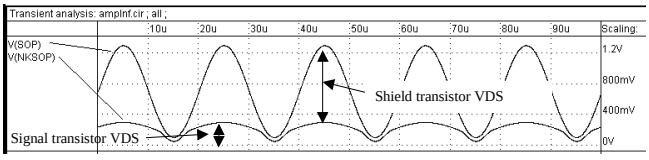

Fig. 5. Shield transistor prevents NMOS from kink.

The final continuous time amplifier right half part with cascode and shield transistors is shown Fig. 5.
Left part, common mode feedback and frequency compensation are not represented :

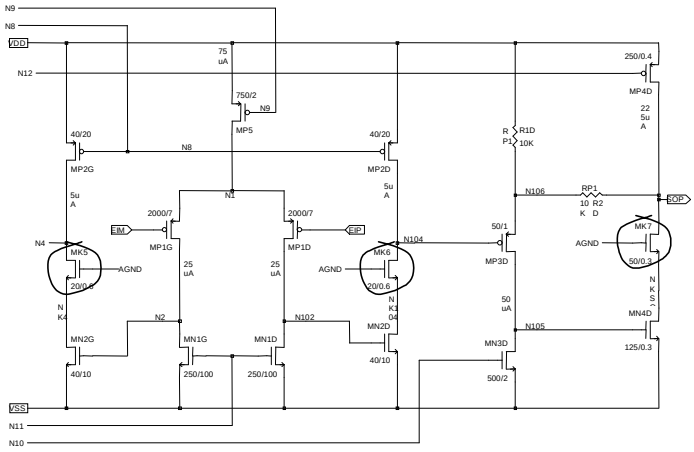

Fig. 6. Continuous time low pass filters amplifier. Circled transistors are dedicated to kink suppression.

2.2 4th order Sigma Delta modulator

Main specifications for the ADC are :

Analog input frequency band = 100kHz, single power supply VDDA = 1.6V to 2.0V, analog sampling frequency = 6.5Mhz. Signal to noise ratio SNR > 78dB (2kHz - 100kHz). Input signal amplitude max = 1.2Vpd

A 4th order modulator is chosen in order to reach a Signal over Noise Ratio of 78dB with an oversampling ratio of 32.

a) Cascade architecture

A 4th order high pass noise shaping may be implemented by several way. For example 2-2 cascade or 2-1-1 cascade.

In a cascade architecture the 3 outputs y_1, y_2 and y_3 are digitally processed within a digital noise cancelling circuitry in order to deliver the net output. These cascaded MASH architecture are widely used but they need a good element matching in order to make precise coefficients, a good amplifier dc gain and settling time.

But this SOI process was developed in parallel with schematics design therefor no accurate data was available.

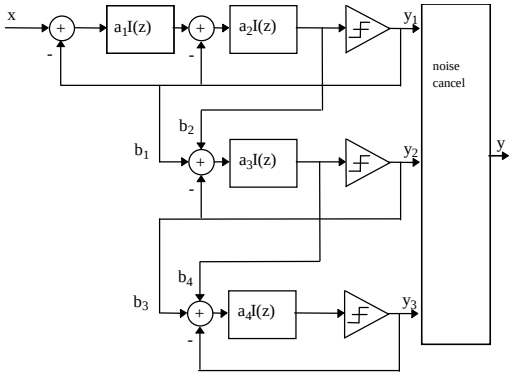

Fig. 7. This cascade 2-1-1 architecture was rejected because of its sensitivity to technological parameters.

b) Single loop architecture

We preferred for our circuit the robustness of the single loop approach. It uses four integrators and one DAC in the feedback path .

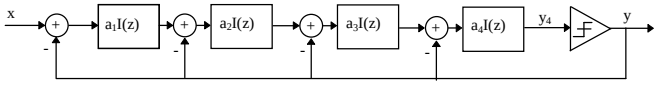

Fig. 8. Single loop architecture. This structure is preferred for its robustness in CMOS SOI

The main design steps of this modulator include the following steps :

1. High level architecture simulation. Coefficients tuning and in-band noise estimation with FFT.
2. First estimation of the modulator flicker and thermal noise.
3. Switched capacitor implementation. Capacitor ratio is given by step 1 and capacitor value is given by step 2, Electric transient simulation with idealized switches and amplifiers.
4. Amplifiers, comparator and phases generator design.
5. Global electric simulation.

We took a rather long time to achieve step 1 because of stability problems. The single loop architecture is conditionally stable and depends on the input signal amplitude. Because higher order (order ≥ 3) modulators may become unstable with high input signal amplitude the output of each integrator must be carefully monitored and each integrator frequency response must be flat in frequency response in order not to lead to an instability with a specific out of band input signal. In this case the instability could be triggered by an internal signal and not by the input signal. For the same reason, the instability may occur at a given frequency and be triggered by an harmonic of the signal. This case may not be detected with a simple single tone signal.

At this stage of the design, the conclusion was that the SNR cannot be satisfied with this structure.

The key parameters for modulator design are stability and Signal/Noise Ratio. SNR cannot be increased by increasing the input signal level because of the low power supply voltage, 1.6Vmin and low voltage reference, 0.8V. So SNR must be increased by decreasing the quantization noise level. This noise level cannot be lowered further by the coefficients values because instability will occur. The only way to decrease noise a step further is to add another output level to the DAC.

As a consequence, a 3 level DAC has been designed :

If y4 ≥ Vthreshold, then feedback –Vref

If y4 ≤ -Vthreshold, then feedback +Vref

If (-Vthreshold) ≤ y4 ≤ Vthreshold, then feedback 0

The final architecture is then :

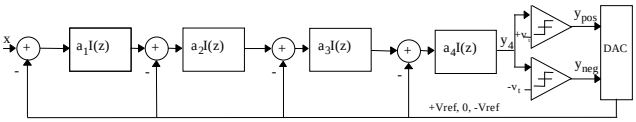

Fig. 9. Final modulator architecture with a 3 levels DAC

c) Coefficients optimisation

The low frequency gain of each integrator is set to unity in order to avoid any clamping or instability within the modulator. For a high Signal/Noise Ratio we must increase $a_1 \times a_2 \times a_3 \times a_4$ but the high-pass noise transfer zeros must not be too close from each other if we want to ensure stability. In a switched capacitor implementation a_i are realized with a capacitor ratio.

d) Modulator amplifier

The amplifier structure used for the integrators is represented Fig.10. The structure is fully differential and has an output common mode feedback. Devices MN3, MN4 form the differential pair which make IHALF to track AGND=0.8V. The feedback signal IHALF is generated with switched capacitors and its value is IHALF=[V(OP)+V(OM)]/2 . The error signal is subtracted to the current bias of the main differential pair in order to bias V(N1), V(N2) to the right voltage.

PMOS current source devices must have high W/L ratio in order to keep them in saturation under VDD=1.6V and with high VTP. Shield transistors are implemented in serie with NMOS MN1, MN2 in order to keep a low VDS . These extra transistors (circled) suppress the small kink on the NMOS drain current for VDS > ≈1V.

The amplifier device size depends on the modulator stage. First and Second stage amplifier are bigger than third and fourth because of noise and load consideration. The modulator's output stage is composed with 2 strobed comparators which form a window detector.

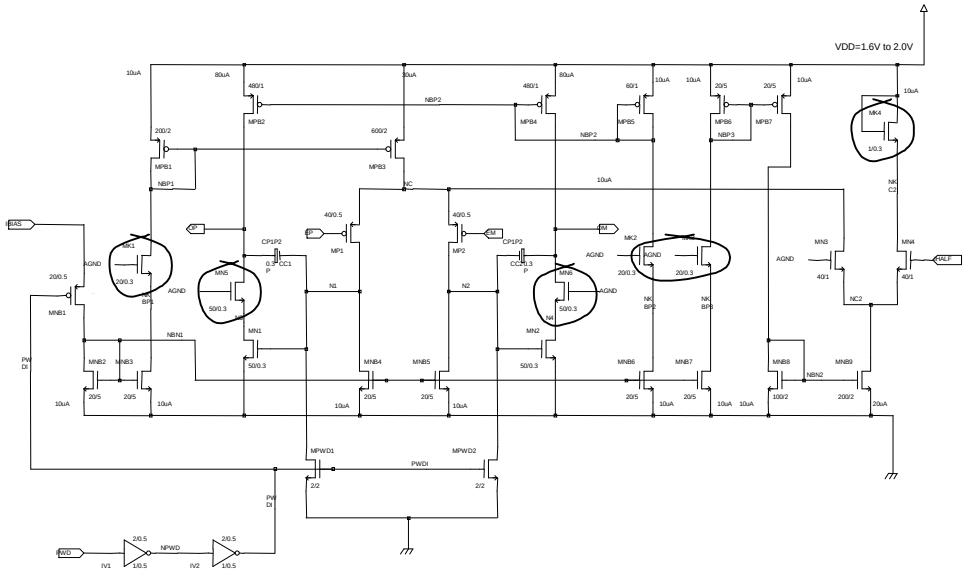

Fig. 10. Fully differential two stages amplifier used for switched capacitor integrators.

3. Silicon measurements

The Base Band circuitry have basically 2 analog differential inputs and 1 digital output displayed on a 14 bits output parallel bus. An input sinusoïdal test signal is applied simultaneously on both I and Q channel. Then it goes through the Low Noise Filter, the Low Pass Filter, the 4th order Sigma Delta modulator and the decimate by 8 digital filter which outputs the signal on the 14bits output bus.

The digital filter output is connected on a PC for performing a FFT for SNR and THD calculation.

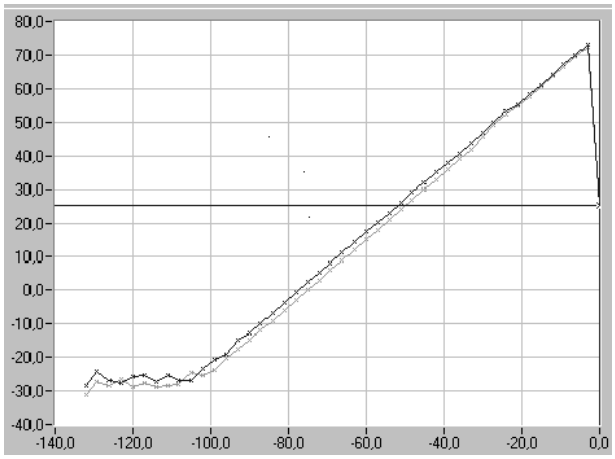

Fig. 11. SNR vs Input Amplitude for I and Q channel. Curves are straight lines indicating that the noise floor is constant down to very low -100dB input signal. Peak SNR is 74dB. Noise measurement bandwidth is 0.9kHz-100kHz.

The base band circuit needs also an external voltage reference of 0.8V a biasing current input of 10uA and a 6.5MHz clock for the modulator and decimator.

On Fig. 11. Are plotted SNR vs input signal amplitude for I and Q channel. Max Peak SNR is 74dB in the noise measurement bandwidth: 0.9kHz-100kHz. 0dB input signal corresponds to 1.6Vpeak to peak differential. If spurious tone had appeared in the band, the slope of the curve would differ from a straight line which is not the case here.

The total base-band power consumption is 13mA for analog part and 5.8mA for digital decimator.

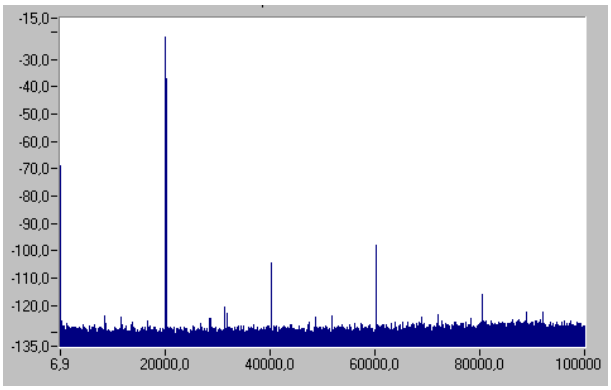

Fig. 12. In band zoom. Input Base Band signal is 20kHz 1.6Vpk-pk differential. Spurious tones excepted harmonics are below -110dB. 65536 points FFT.

4. Conclusion

Some methods to cancel kink effect in fully depleted SOI process have been described. Silicon measurements on this single chip receiver show good analog performances in continuous time and switched capacitors circuitry.

These results make SOI a good candidate for low power mixed signal circuits.

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