A -100 dB THD, 120 dB SNR programmable gain amplifier in a 3.3 V, 0.5µm CMOS process

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ABSTRACT.

A fully differential amplifier that operates from a 3.3V±10% power-supply and featuring a -100dB THD at 2Vpp output voltage was realized. Equivalent input noise in the 100Hz - 10kHz audio-band is 4tVrms, leading to a 120dB SNR. This amplifier is used as the core of a programmable gain cell in the front-end part of a A AID converter. The good linearity performances are achieved thanks to a novel low impedance output stage which uses a simple but efficient schematic allowing rail to rail operation on a resistive and capacitive load. Such low distortion performances actually surpasses most available test equipment and the last section explains how to deal with that fact. The technological process is 0.5tm double poly CMOS from the « centre commun »
CNET-SGS-THOMSON at Crolles, France.

I INTRODUCTION.

Widespread use of high performance ∑Δ A/D converters has increased the need for front-end circuitry for analog signal conditioning. Digital part of ∑Δ fully exploits the new advances of digital technologies, and it is a hard task for analog part to meet ever greater performances with decreasing power-supply voltage. A programmable gain amplifier was realized in that context. Its voltage gain range is from -20dB to 20dB by 0.5dB steps and it has to meet simultaneously low power consumption, very low noise and 3V power-supply constraints.

II CIRCUIT DESCRIPTION.

Several approaches were considered. A differential difference amplifier solution [1] presents a high input impedance but exhibits weak linearity performances. The realisation described in [2] uses bipolar devices and is not applicable to 3V power-supplies. We have chosen a full CMOS approach for the amplifier and a differential resistor string with logarithmically spaced taps for voltage gain programming. Among non inverting and inverting configuration, inverting topology was prefered for low distortion and low voltage power-supplies. In this configuration common mode voltage is removed from the opamp input differential pair, thereby keeping the bias current of the input pair constant. The low noise requirements, 1µVrms in the band 100Hz-10kHz, dictates rather low input and feedback resistors, in the lkΩ-lOkΩ range, leading to an important loading effect for the output stage. A low impedance output stage in then mandatory to ensure

constant accuracy and speed for load changes with programmed gain. The 3V power-supply dictates a common-source output stage with local feedback because a simple follower cannot be used any more in 3V technology. The new output stage that has been developed exhibits linear rail to rail operation.
The core amplifier schematic is composed of 3 main blocks
A) Input differential stage, B) New output stage and C) Frequency compensation.

A) Input differential stage. PMOS input pair is prefered for its lower 1/f noise (figure 1). The load is active in order to realize a high gain voltage with two stages only. By this way, the frequency compensation is simplified. Therefore, we did noise optimization only on this first stage because the noise voltage of the following stages is divided by the first stage voltage gain. Guidelines for low I/f noise are given by [3] :

$$e_n(in) = \sqrt{\frac{\alpha}{w_{mp1} l_{mp1}}\left[1+\frac{\beta}{\gamma}\left(\frac{l_{mp1}}{l_{nn1}}\right)\right]}$$

which leads to the following rules

- High aspect ratio for input devices.
- Long channel active loads.

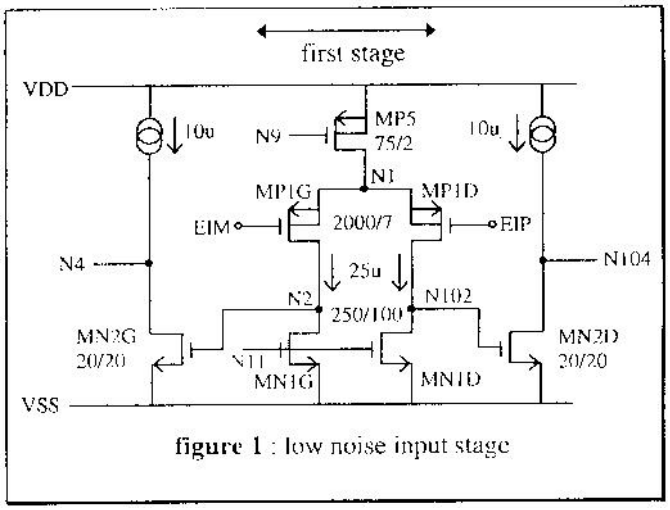

figure 1 : low noise input stage

The important fact here is that active loads MN1G and MN1D being static devices, there is no tradeoff between low 1/f noise requirements and speed. Therefore MNID and MN1G are very long channel devices. However W/L ratio is kept reasonable in order to insure a goon saturation margin lor voltage gain provision.

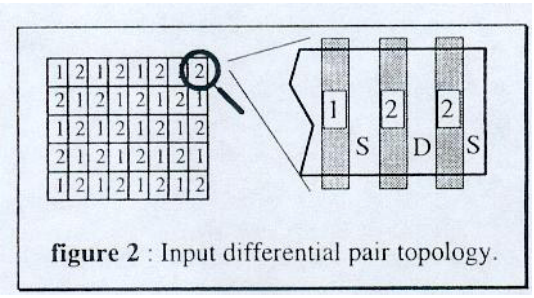

figure 2 : Input differential pair topology.

Differential input/output amplifiers require a common-mode feedback circuitry which forces the output of the whole amplifier to be centered around VDD/2. This is done by sinking or sourcing some amount of current to or from node N1 (not represented in the schematic figure 1). The second gain stage is built with a common source NMOS biased at a constant l0µA drain current. Low W/L ratio and bias current will be justified later.
Noise contribution from the biasing stages appears in common mode on nodes N2 and N102 and it is cancelled by the differential topology. Cancellation is effective only if perfect symmetry is respected in the layout of the four devices MP1G, MP1D, MN1G, and MN1D. In this case, optimum noise performances predicted by simulations can be reached.
These four critical devices are laid out in such a way that drain and source remain identical even for non perpendicular ionic implantation of drain/source area [4]. Figure 2 represents the input pair layout were each 2000/7 device is cut into 40 elementary back to back 50/7 transistor. NMOS active loads follow the same layout strategy.
Good electrical symmetry is also profitable for the structure offset, which is rather low for a CMOS process. Offset measurement results are displayed in section **III**.

B) Output stage. A special effort was spent on this part of the cell (figure 3). The need for a local feedback means that one must be able to sense the output voltage from rail to rail and to compare it to the input signal (or to a replica of the input signal). This is done through a current feedback loop. This output stage displays a voltage gain of 2 and uses a class A output branch. The local feedback linearizes the dc transfer function of the output stage and reduces the output impedance. Linearization improves overall THD and low output impedance provides speed and low sensibility to variable load. Compared to the main loop around the amplifier this local feedback is very fast and thus is well suited for switched load. The ac small signal voltage gain is given by :

$$\frac{v(sop)-v(n104)}{R2}=\frac{+v(n104)}{R1}$$

(the current through MP3D is assumed to be constant). Then

$$\frac{v(sop)}{v(n104)}=1+\frac{R2}{R1}=2 \text{ because } R1=R2$$

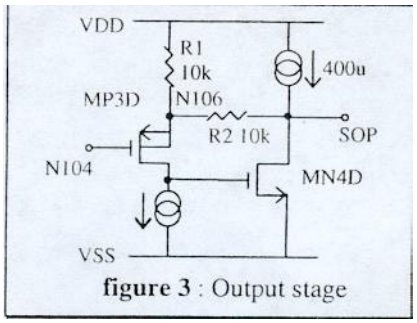

figure 3 : Output stage

C) Frequency compensation. The amplifier and its output stage are represented on figure 4. (Only the right half part is depicted for clarity purpose). Prior to frequency compensation, the output stage dominant pole is located on MN4D's gate and has to be slowed down. Capacitor CC2D is added to move this pole toward lower frequencies. Compared to a Miller capacitance connected between gate and drain of MN4D this frequency compensation is more efficient because the capacitance effect is magnified by a factor equal to CC2D/Cgs(MN4D). The purpose of CC3D is to cancel the time constant R2xCC2D.

The whole amplifier is stabilized with the capacitance CC1D=2OpF. CC1D could have been connected between N102 and Nl04 but this would lead to a high gm for MN2D because it would have been necessary to move the pole located on node N104 toward high frequencies. High

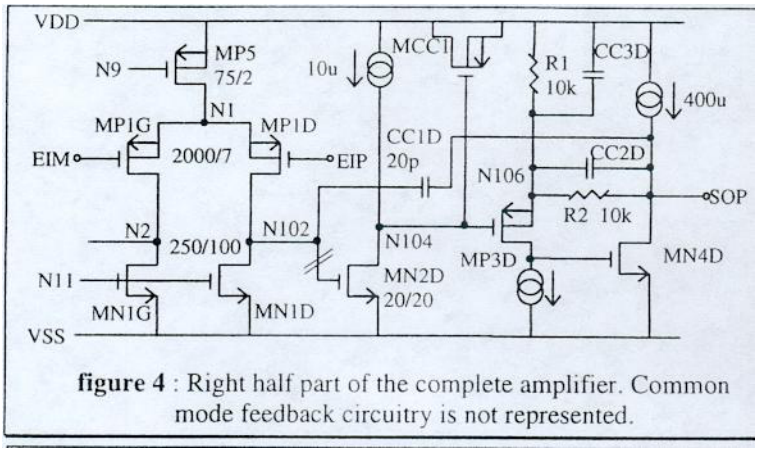

figure 4 : Right half part of the complete amplifier. Common mode feedback circuitry is not represented.

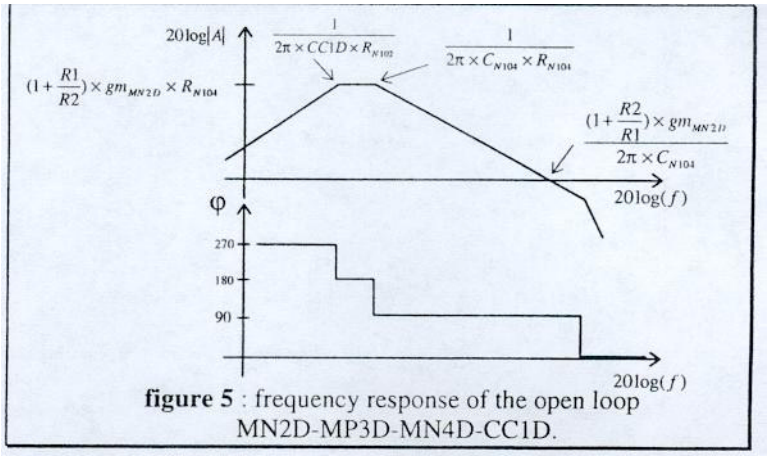

figure 5 : frequency response of the open loop MN2D-MP3D-MN4D-CC1D.

gm for MN2D would decrease gain and linearity. The actual compensation can be studied by disconnecting MN2D from N102 (at point marked with //) and applying a signal generator on the gate of MN2D.

The frequency response of the loop MN2D-MP3D-MN4D-CC1D is shown on figure 5.
Stability increases if gm(MN2D) is decreased and/or capacitance on node N104 is increased. This explains the small size and low bias current of MN2D and gate capacitance MCCI. When the loop is closed, the whole amplifier frequency compensation is similar to a standard two stages amplifier.

III EXPERIMENTAL RESULTS.

Three kind of measurements were performed 1) Equivalent input noise and offset, 2) low frequency open-loop gain and 3) Output total harmonic distorsion.

1) Noise and offset are mesured with a gain of 1000 in inverting configuration (test circuit showed in figure 7 with Rl=R2=lkΩ and R3=R4=1MΩ). This method raises the amplifier noise level above test equipment noise threshold. Total offset is measured at the output and divided by 1000. Output noise is mesiired in differential mode, between SOP and SOM outputs with a differential input spectrum analyzer. Figure 6 shows the measured differential output noise, amplified by 40dB.

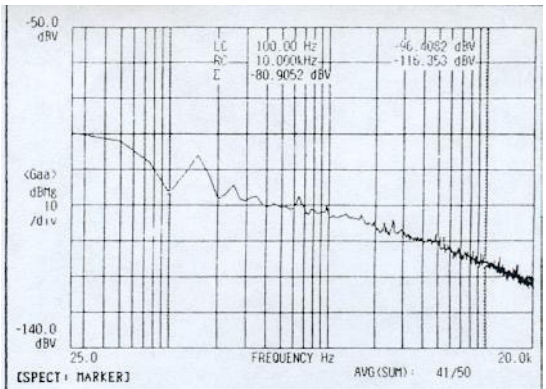

figure 6 : Noise measurements.The noise band is defined by left and right markers LC and RC. Total noise is Σ=-81dBV. Taking into account for probe attenuation -20dB and feedback resistive network +60dB lead to a total input refered noise of

$$N = -81dBV - 60dB + 20dB = -121dBV = 1.1\mu V_{rms}$$

2) Low frequency open-loop gain is measured in two steps using a setup similar to figure 7 with Rl=R2=R3=R4=10kΩ. We first measure the output amplitude and then the input amplitude EIM-EIP. Amplifier open-loop gain is given by the ratio of these two results.

3) Distorsion measurement is challenging because it actually surpasses most test equipments performances.

The method described in [5] explains the way to cope with that fact by measuring the amplifier input error signal instead of the output, and the way to correct the results to get output refered distorsion.

Sinusoidal differential input signal is applied between inputs EM and EP (figure 7). The first step is to connect the differential spectrum analyzer to the generator outputs EM and EP and to estimate the amount of generator's harmonics components present on the amplifier inputs ElM, EIP. For that, we divide each input harmonic magnitude by the amplifier open-loop gain at this frequency.

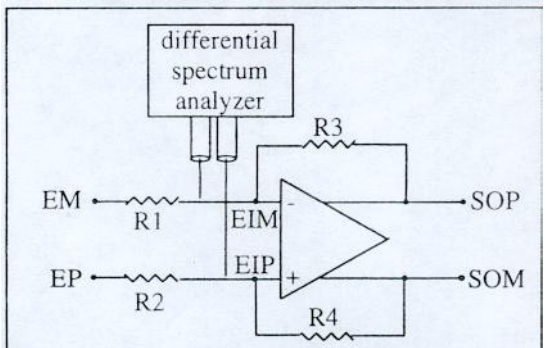

figure 7 : experimental setup for offset, open loop gain and THD measurements. Input refered THD measurements reduces signal generator distorsion effects and dynamic range required for the spectrum analyzer.

The second step is to connect the let analyzer right on ElM and EIP and to observe the frequency spectrum. If the harmonics magnitude are higher than those calculated during first step then we

are actually measuring the input refered amplifier distorsion. The third step is to multiply the total harmonics power by 2 (because noise gain is 2) in order to obtain the amplifier output THD. Experimental and simulated results are summerized in figure 8.

IV CONCLUSION

A low noise and low distorsion fully differential amplifier for gain setting in the input stage of a ΔΣ A/D converter has been realized in a 0.5µm, 120Å gate oxyde, 2 poly, 3 metal and 3.3V CMOS technology. is T the first time that such level of performances, -100dB THD and 120dB SNR are reported in a 3.3V process.
Experimental results were difficult to collect and a special effort has been done to carry them through.

VDD=3V. T=amb.	measured	simulated [6]
DC gain	100dB	97dB
offset (5 samples)	30µV-288µV	0
THD @ 1kHz †	-100dB	< -113dB
noise 100Hz-10kHz	1.1µVrms	1.2µVrms
power cons.	1.3mA×VDD	1.3mA×VDD
area††	0.24mm2	

† 10 harmonics included
†† amplifier alone

figure 8

Acknowledgments
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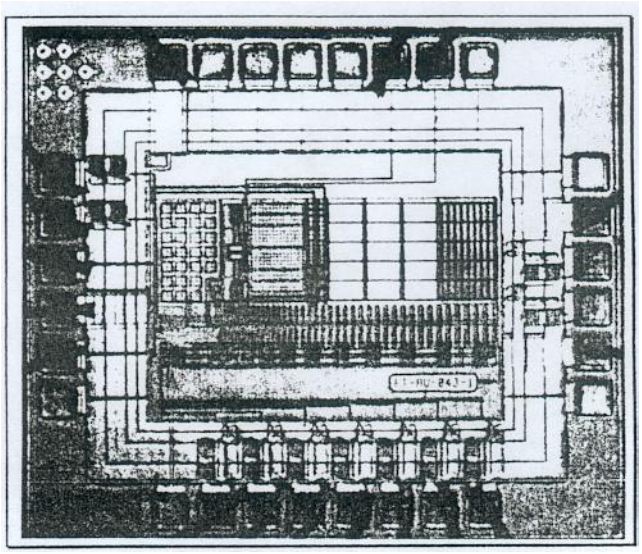

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