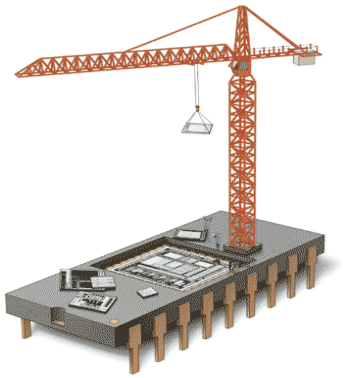
A real « softness » of mixed signal « hard » Virtual Components



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DesignCon 2000 - Jan.31-Feb.3- Santa Clara

There are some paradoxes in the SoC industry. Here is the crux of the matter for the analog and fast electrical parts: Innovative products involving SoC development often require usage of the latest technological process, together with a mix of high performance logic and analog functions. Reducing cost, time and risk of SoC designs requires the re-use of Virtual Components. Well, re-use clearly means that such functions have already been used and this is the paradox when analog parts are involved because analog functions are always different from one application to another one and they have to be retargeted and tuned for each process.
The challenge then is to offer solutions coping with these constraints.

Overview

- Design requirements for Analog and Mixed Signal (AMS) Virtual Components (VC)
- Examples: PLLs and high resolution ADCs
- Flexible solutions to efficiently achieve the design: CSK and ADMIR
- Methodology for Analog Retargetability
- Retargetability of schematics and layout
- Conclusion

This presentation will first review the challenges currently met in analog design and will show that better than a full catalogue of fixed functions, a methodology based on basic hard cells, kits and generators together with an efficient retargeting methodology may be a soft answer to a hard problem.
- In a first section, the main design requirements for Mixed Signal Virtual Components will be described
- The next section will illustrate, through two examples of PLL and two examples of high resolution ADC issued from real applications, the wide range of requirements encountered in SoC design et why it is necessary to have a design methodology offering flexible solutions
- The third section will show how we have implemented such a methodology for PLLs and high resolution converters: a Clock Synthesizer Kit for PLLs based on loose cells, namely CSK, and a Generator of Analog to Digital Converters for ADCs, namely ADMIR
-The two following sections will adress the retargeting methodology we apply for analog functions. This retargeting methodology is twofold: retargeting of analog schematics and retargeting of layout
We will finally come to a conclusion with some promising perspectives and trends

Challenges for SoC design including AMS VCs

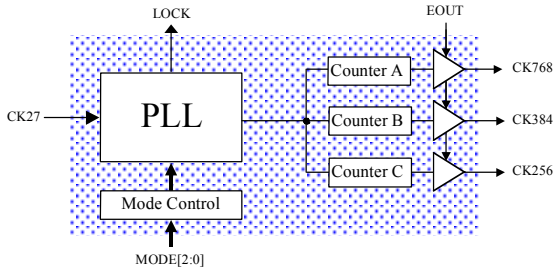
- **Time To Market**
- **SoC right on first pass**

  -> VCs with a high IQ (Indice of Quality)
- **To be able to choose**
  - **the manufacturer, the technological process, a second source**
  - **While maintaining performances, yield and reliability**
- **To be able to provide a function or performances matching the application's needs**
  - **E.g. functionality, power consumption, resolution…**

What are the challenges of SoC design including Analog and mixed signal VCs?
On the logic side, HDL languages offer the possibility for designing complex logic functions while remaining independant from the technological fabrication process until an advanced stage in the SoC design flow: HDL-based models of VCs are ready-to-be-used and re-used, whatever the fabrication process, offering solutions often compatible with Time To Market requirements.
But analog functions (or high speed logic functions) have to be delivered as hardware VCs, because their performances can be guaranteed only after carefull tuning and checking through detailed design rules and transistor characteristics of the targeted process.
Moreover, the differences in requirements from one application to another one always need modifications of some functionality or characteristics making a catalogue of fixed pre-defined and reusable functions an irrealistic dream or nightmare: Ready-to-be-used or re-used analog VCs available in the right process, with the right performances are an illusion.
All these issues, specific to AMS VCs, add to the usual SoC design flow new challenges:
- The retargeting methodologies from one process to another one has to be compatible with the Time-to-market requirements
- The design process for modifying the functionality and perfomances of a given VC has also to be compatible with the Time-to-market requirements
- The capability of choosing different processes for various reasons has to be offered
-The capability of mixed signal and multi-level simulations at different steps of the SoC design is necessary
All these requirements have to be fullfilled with a high level of quality implying bug-free, reliable solutions and high production yields.

Example 1 - PLL

Clock generator for MPEG audio applications



CHARACTERISTICS

- generated **audio system clock signals** 256×Fs, 384×Fs and 768×Fs
- **multiple output sampling frequency**: Fs = 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz
- Single input frequency: **27 MHz**

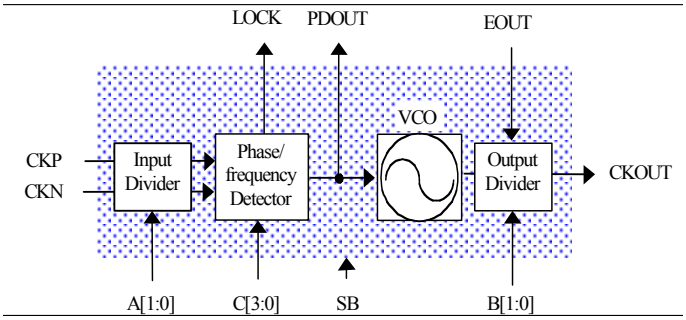
FEATURES

- single power supply: **+1.8V to 3.7 V**
- power-down mode
- internal loop low pass filter
- retargetable towards any deep submicron CMOS process

The first example is a PLL dedicated to MPEG audio applications. The main requirements for this PLL are the following ones:
- one fixed frequency input clock signal at 27 MHz, corresponding to a commonly used quartz crystal
- three outputs clock signals, corresponding to several possible output frequencies used in MPEG audio applications:the PLL has to be able to deliver 256Fs, 384 Fs or 768Fs clock frequencies where Fs can be chosen among different values commonly used in audio applications between 32 kHz and 96 kHz
- the complete analog and logic circuitry have to be fully integrated, including the loop filter

Example 2 - PLL

Analog Front End for Clock Synthesis



CHARACTERISTICS

- **Programmable output frequency from 5 MHz to 250 MHz**
- **Input frequency**: up to **250 MHz**
- **Low Power Consumption**

FEATURES

- single power supply: **+1.6 V to 2.75 V**
- power-down mode
- external loop low pass filter
- retargetable towards any deep submicron CMOS process

This second example is the analog part of a PLL dedicated to cover different clock synthesis applications with various characteristics. This analog front end has to be put in an ASIC library; it has to cover a large working area for input frequencies and output frequencies with the following main features:
- Power supply voltage between 1.6 V and 2.75 V in a 0.25 µm CMOS process
- Input frequency range between some kHz and 250 MHz
- Output frequency range between 5 MHz and 300 MHz
- Maximum cycle to cycle jitter depending on the output frequency, e.g. 150 ps for Fout = 128 MHz
- Due to the large working area, a single loop filter cannot be used ; it has to be designed for each application and depending on the requirements, it may be integrated on the chip or remains external.

The requirements of this example are different from the previous one: larger range of input-output frequencies.
We will show later in this presentation how we can cover both examples with the same design methdology and kit of cells.

Example 3 - ADC with multiple inputs

- Application: Electronic Circuit Breaker
- ADC with Multiple analog inputs:
  - 4 single ended inputs with 13 bits DNL and INL, 2 kHz sampling frequency, with input signal between 500 µV and 1.2 V
  - 3 differential inputs with 11 bits DNL and INL, 2 kHz sampling frequency, with input signal between 100 mV and 1 V
  - 1 differential input with 13 bits DNL and INL, 2 kHz sampling frequency, with input signal between 10 mV and 1 V
  - 1 differential input with 6 bits DNL and INL, DC
  - 2 single ended inputs with 6 bits DNL and INL, DC
  - Low power consumption
  - Offset cancellation for each analog channel

We will describe now shortly two examples of applications requiring Analog to Digital Converters. We concentrate on applications with high resolutions, higher than 10 bits, with sampling frequency between DC and 100 kHz. Typical applications are sensor interfaces, automotive, power management, data acquisition.
The first application is for an electronic circuit breaker. This application requires the conversion in digital of several analog signal with various characterstics: conversion of current and voltage inputs, conversion of temperature value and other data coming from. different sensors.
The typical requirements are mentionned on the slide:
- 4 single ended input with 13 bits DNL and INL, 2 kHz sampling frequency, with input signal between 500 µV and 1.2 V
- 3 differential inputs with 11 bits DNL and INL, 2 kHz sampling frequency, with input signal between 100 mV and 1 V
- 1 differential input with 13 bits DNL and INL, 2 kHz sampling frequency, with input signal between 10 mV and 1 V
- 1 differential input 6 bits DNL and INL, DC
- 2 single ended 6 bits DNL and INL, DC
- Low power consumption
- Offset cancellation for each analog channel

Has to be designed in a 0.35 µm pure logic CMOS process

Example 4 - ADC

- Application : general purpose 10 bit ADC
- E.g. used in voice digitization:
  - One channel
  - Single ended or differential input
  - programmable sampling frequency
  - example of characteristics required at Fs = 8 kHz
    - Single ended input
    - INL < ± 0.1%
    - Low power consumption (< 2 mA)
    - Small silicon area

This second example is to be used in an ASIC library and can covers different applications like voice digitzation, data acquisition or sensor interfaces.
It is different from the previous example: if the number of analog channel is only one, this channel has to be programmable, it means that the user may have the possibility to choose between a single-ended and a differential input and also, the sampling frequency may be programmed.
The resulting Virtual Component had to respect some characteristics mentionned on the slide for a sampling frequency at 8 kHz. It corresponds to a first usage of this VC in an application for voice digitization.
The ADC had to use a single ended input with INL < ± 0.1%, a power consumption lower than 2 mA and a silicon area as smallest as possible are required.
It had to be designed in a 0.35 µm CMOS 3.3 V pure digital process
Like for the PLL examples, we will show later in this presentation how we can cover both examples of ADC with the generator we have designed.

What is the solution?

- Off-the-shelf Products? **Unrealistic**
  - Would require a full range catalogue
    - too many processes, too many functions
- The solution? **K.L.A.M.S**

  Kits for **L**ogic **A**nalog **M**emories and **S**ervices
  - A **Kit of basic cells and generators**, ready to be retargeted
  - An efficient **methodology for retargeting**:
    - Quality, guaranteed performances, short retargeting time
  - A capability of **tuning existing solutions to application needs**
    - Competences and reactivity of the design team

As illustrated by the four examples, and we could find a lot of other examples, the requirements of the applications are so different that if you want to provide efficient solutions for each case with a high level of quality, it is impossible to have off-the-shelf products. Off-the-shelf products would require a full-range catalogue with a extremely high number of functions. Moreover each product should be available in a lot of different technological processes (0.5 µm, 0.35 µm, 0.25 µm and so on) from different foundries or semiconductor manufacturers. Unrealistic

An alternative would be to have completely programmable functions; unrealistic too: it would require a lot of time and resources to design such programmable functions and to characterize them, and it would lead to unacceptable features like silicon area, power consumption…

So, what is the solution?

We call it KLAMS at Dolphin. KLAMS stands for Kit for Logic Analog Memories and Services.

What does it mean?

It means that for a family of functions, for example PLLs, ADCs or Memories, we have a kit of generators, loose cells, architectures allowing us to cover a wide range of technical characteristics.

Together with these kits, we have developed an efficient methodology for retargeting these functions to different CMOS processes, to be able to guarantee short delays of deliveries and a high level of quality and high production yields.

Flexibility through generator and kits of cells

- « **Hardware** » Analog and Mixed Signal VCs benefit from the « **softness** » of the methodology for building them, and matching the requirements of each application

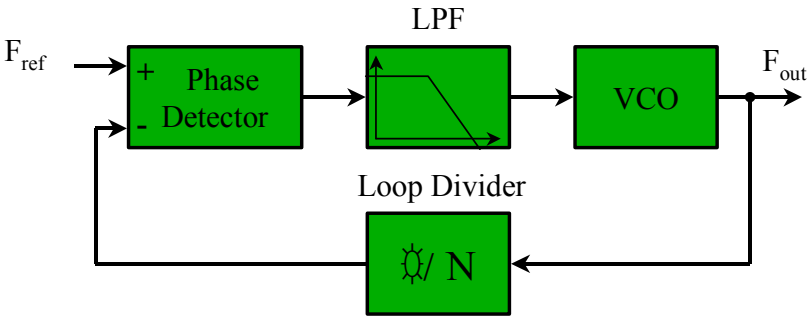
- Two examples
  - **CSK**, Clock Synthesizer Kit for building PLLs
  - **ADMIR**, a generator of high resolution ADC

Analog and Mixed Signal Virtual Components are hardware Virtual Components but we build them with a methodology whose softness allows match ing the requirements of each application.
To illustrate this approach, we will now have a look at the answer we provide for the examples previously described, the PLLs and the ADCs.
For PLLs, we use a kit of loose cells called CSK standing for Clock Synthesizer Kit.
For ADC, we use a generator of high resolution ADCcalled ADMIR.

CSK : Clock Synthesis Kit

- **Kit of loose pieces**: VCO, Phase Detector, Loop Divider…)
  - for building **customized solution** for applications like:

Clock generation for processor, sigma-delta codecs, video pixel...

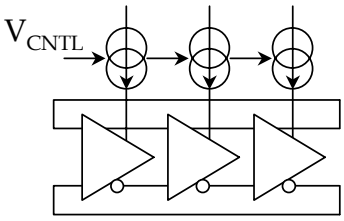


The approach here is based on flexible basic cells.
Before looking at the working area of the PLL covered by this family of basic cells, let us just have a look at the general architecture of a PLL.
The main blocks are a phase detector, a loop low pass filter, a VCO and a loop divider.
Each of these blocks may be designed with different approachs, each approach having its own advantages and drawbacks and the choice of a solution between each architecture will be driven by the requirements of the application.

VCO Architectures

1
1

Ring Oscillator



Advantage and drawback:

☺Ease IC-integration

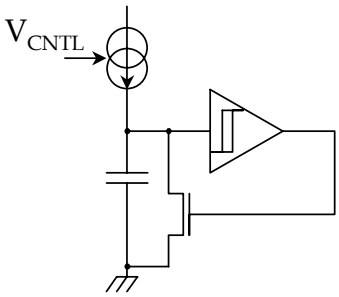
☺ High Frequency

☹ Bad Phase Noise

Use:

High Frequency Clock

Multivibrator



Advantage and drawback:

☺ Ease IC-integration

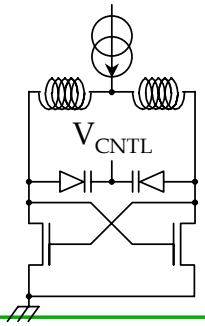
☺ Large Frequency Range

☹ Bad Phase Noise

Use:

Clock Synthesis

Resonant Circuit



Advantage and drawback:

☺ Low Phase Noise

☹ Narrow Frequency Range

☹ Difficult to integrate

Use:

RF Synthesis

Take the example of a VCO. Several designs may be used. Three main ones are summerized on the slide. Please note that advantages and drawbacks are relative and not absolute.

The advantages of the ring oscillator approach are that it allows to target high frequency and is easy to implement in an Integrated Circuit without external components. To give some ideas, we can generate clocks in the range of 200 MHz to 500 MHz in 0.5 µm CMOS processes. Such a VCO will be used for the generation of high speed clocks but not only.

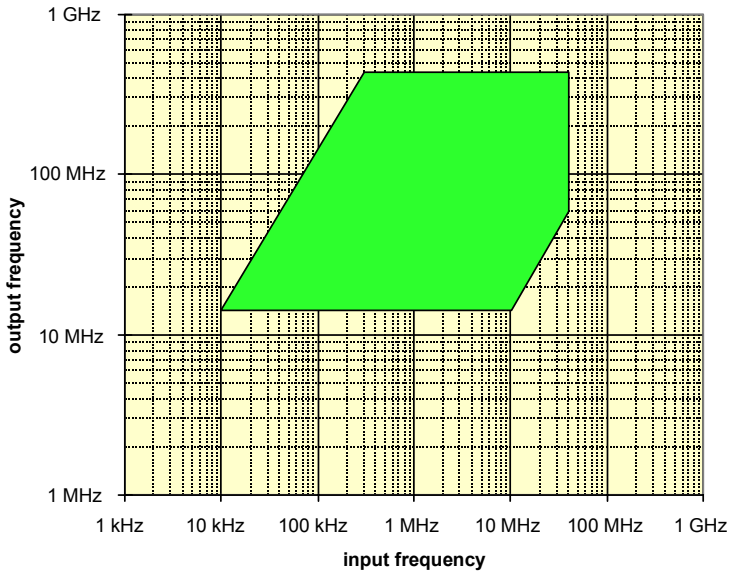
In comparison, the multivibrator approach offers a larger range of output frequencies but with a lower maximum frequency and the same range for the jitter. It can also be easily designed in an Integrated Circuit. Once again, it will be posible to generate output frequencies in the range of 10MHz to 300 MHz in 0.5 µm CMOS processes. It will be used for clock synthesis systems. But be carefull, greater is the output frequency range covered by the VCO, greater will be the jitter.

The third solution is the use of a resonant circuit. Such a solution is more difficult to integrate due to the presence of selfs. Selfs may be external or internal but internal selfs are often not characterized by the manufactuer and require a first test chip for adjustment. In fact, the values and accuracy required for the self will depend on the targeted frequency.

Typically self in the range of 1nF to 15 nF are integratable and allow output frequency ranges between 700 MHz and 2 GHz with acceptable silicon area. As an the silicon area of a 10 nH self will be less than 0.03 mm2. External self will be uses for lower frequencies, less than 500 MHz. Moreover, for such frequencies self of bonding wires Imay be neglected. The main advantage of this architecture is a low phase noise and the drawback is a relatively narrow frequency range. In 0.5 µm CMOS processes, the maximum output frequency will be in the range of 850MHz to 950 MHz. This solution is used for RF synthesis.

The VCO architecture chosen for our Clock Synthesis Kit is the second one.

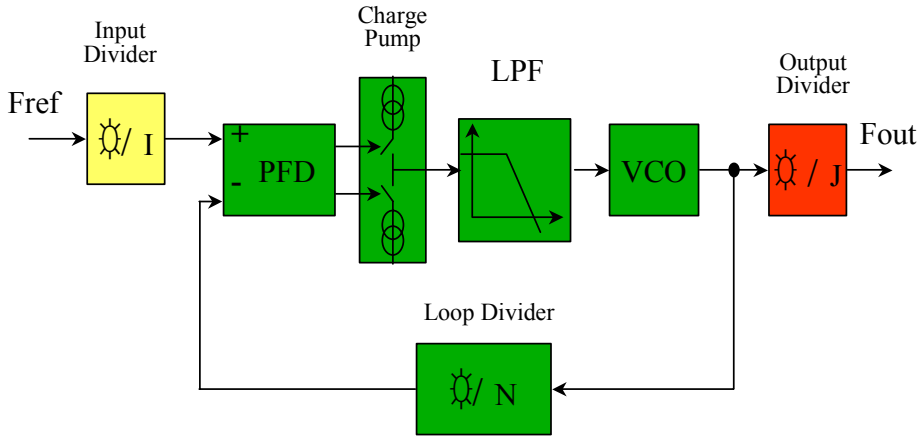
CSK Working Area in 0.35 µm



Have a look now on the next slide. It corresponds to the working area of our Clock Synthesis Kit.
This working area is given for a 0.35µm CMOS technological process with a power supply voltage range between 1.8 V and 3.6 V.
For a given application, the characteristics to discuss will be the output frequency range, the power supply voltage range, the maximum power consumption, the maximum jitter and the maximum locking time.
When changing the technological process towards deep submicron processes, 0,25 µm, 0.18 µm and so on, the working area will move, offering higher output frequencies.
The upper and lower borders of this area are due to the VCO ’s maximum and minimum operating frequencies; the maximum input frequency represented by the vertical border on the right side is due to the maximum frequency of the phase detector and the two oblic borders are due to the minimum and maximum values acceptable for the loop divider.
The green working area is obtained with a set of only one VCO, one Phase detector and one loop divider architecture. But the schematic of each VCO cell is tuned for achieving the performances required by a specific application and the schematic principles of the loop divider may also be chosen depending on some application features.

How to Extend the Working Area

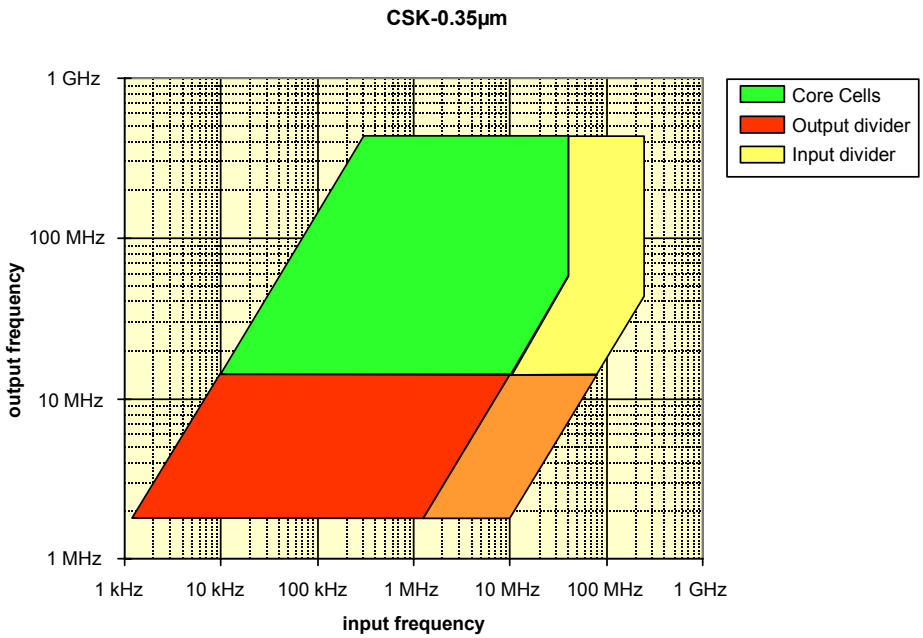
13



Fout = Fref x N / (IxJ)

Another interest of this approach is to be able to deliver PLLs not only in the working area, but also to be ready to propose a solution if the requirements of a specific application are not in this working area.
How can we achieve that ?
The working area may simply be extended by adding a divider on the input and a divider on the ouptut as described on the slide.
What are the limitations of this approach:
A- Addition of an output divider
The only drawback of the usage of such a divider compared to an optimised PLL is the power consumption. In fact, it obliges the VCO to work at higher speed, so to have higher power consumption; the divider itself will have a higher power consumption for high input frequencies.
The advantage of an output divider is to reduce the jitter, following a square of N rule where N is the divider ratio.
B- Addition of an input divider
The drawback here is the power consumption and the jitter. The jitter is higher when the phase detector works at a lower frequency, which will be the case if the re is an input divider. The power consumption of the input divider may be significant, roughly equivalent to the VCO itself, because the input frequency of this divider may be very high. Moreover, such dividers with high input frequencies are sometimes not available and have to be designed specifically.
When such consequences are known and understood, the choice of the solution tuned to the application needs may be done.

CSK Extended Working Area



A typical extension of the working area is shown on the slide.

How do we manage the design of a PLL for a new application?
When the working input and output frequencies are fixed, the purpose is generally to reduce the jitter to a minimum value.
To achieve that,
- first we try to be as close as possible of a divider ratio of N=1 for the loop divider.
- second, the VCO output frequencies have to work in the smallest range as possible. The VCO design allows to do that by a tuning of some resistors values.
The phase detector cell is a fixed one, operating up to 40 MHz and covering all the encountered applications until now. In the future, with the increasing frequencies, another phase detector cell can be easily designed.
For the loop divider, two solutions are available:
- a swallow counter, which can generate almost every divider ratio, even fractional ones
- a pseudo-random divider
The differences between the two solutions are relative to the noise: the swallow counter generates spurs which can be acceptable or not, the pseudo-random divider generate noise, spread on the frequency spectrum. The applications requirements will allow to choose the best suited solution.

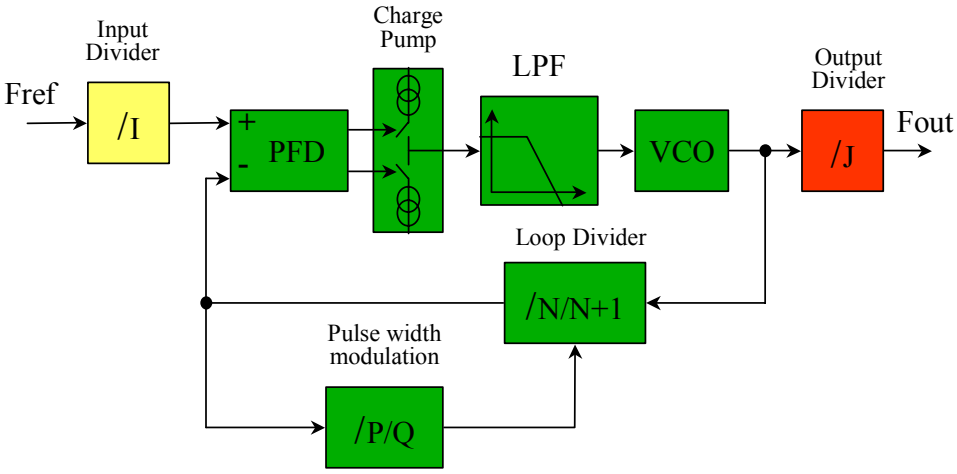
CSK Benefits

- Wide working area
- Quick delivery time
- Easy improvement
- Pure logical CMOS processes
- Possible extension of the methodology

Other important characteristics of this CSK design and methodology have to be mentioned
A- use of pure logic process
Our basic cells and overall design of the PLL do not require analog characteristics for the process: no need for special resistor or capacitor layers. Nevertheless, some capacitors and resistor are used. The capacitors have not important values and are realized as transistor capacitors and resistors use the NWELL layer.
B- Retargetability of the layout
The constraints for retargeting a PLL are different compared to the retargeting of an ADC as the one previously described. Indeed, one of the most important issues in the design of a PLL is the frequency. It means that the design may be very sensitive to parasitic loads, typically drain area of transistors or interconnection parasitic capacitance. In this case, the retargeting procedures has to be carefully studied to take this constraint into account.

In summary with the CSK approach:
- we are able to deliver a PLL solution within some weeks if applications requirements are in the working area previoulsy described
- we are able to answer within some days to the feasibility of PLLs outside this working area
- thanks to our methodology of portability, we can offer the shortest possible delivery time, even in case of a PLL outside the working area
- the working area may be extended or modified by simply adding new basic cells
- An easy and efficient retargeting can be done towards any pure logical CMOS processes
- This approach may be also employed for PLLs covering other applications types like RF.

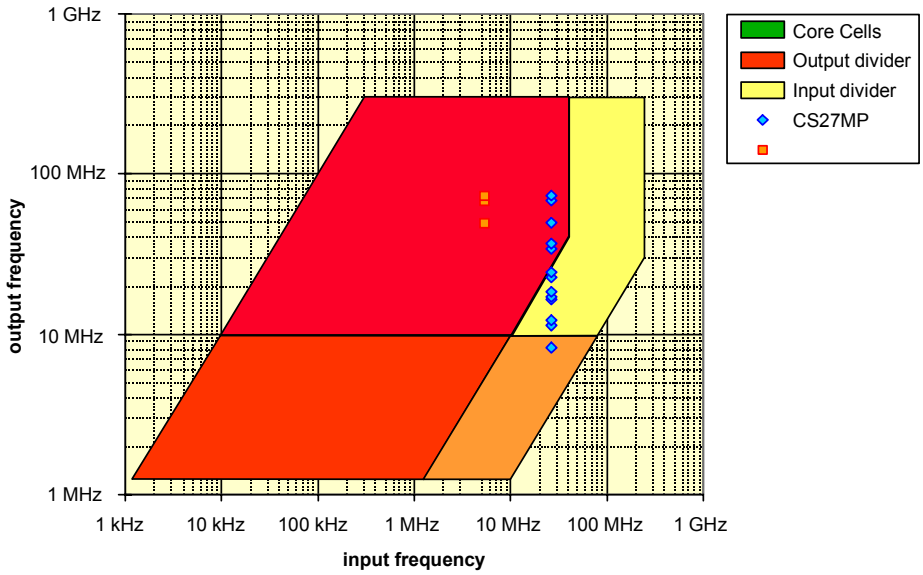
CSK applied to example 1



$$F_{out} = (NxQ+P/IxJxQ)F_{ref}$$

Remember the main features of the example 1: a fixed input frequency at 27 MHz, several output frequencies to fullfill the requirements of various audio sampling frequencies between 32 kHz and 96 kHz with the capability of generating oversampled freqnecies at 256 Fs, 384 Fs and 768 Fs.
The generation of all the possible configurations of the output frequencies is achieved thanks to two flexibilities of the kit of loose cells:
- firstly, a highly programmable logical parts, including several programmable dividers, some of them fractionnal as described on the slide

CSK applied to example 1

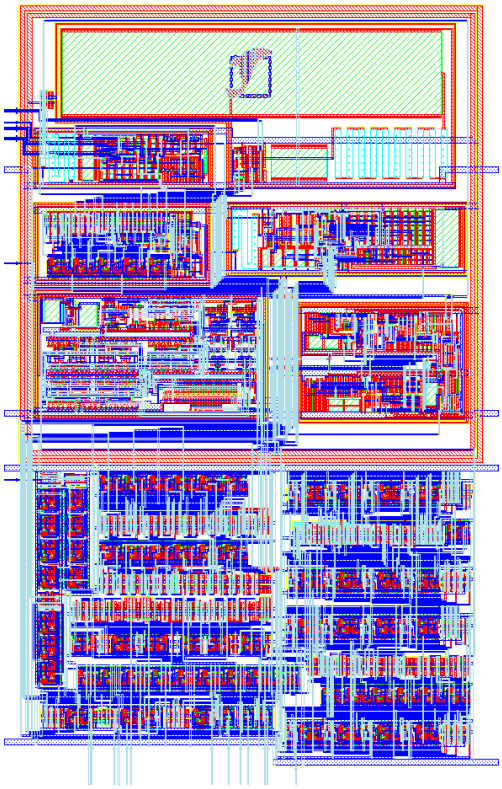


- Secondly, the VCO frequency may be programmed for oscillating at three different frequencies between 49 and 73 MHz. This is necessary for generating the 13 different output frequencies required by the application. The slides shows in red colour the frequencies of the VCO and in blue the 13 output frequencies of the PLL.
The control part of the PLL drives the different counters and dividers and also programs the VCO at the right frequency by selecting internal resistors values.
This design allows to fulfill an important requirement of this application: to generate output frequencies with exact frequencies values, without offsets!
The resulting Virtual Component is working between 1.8 V and 3.6 V.
- The typical performances reached with a 0.35 µm process is a power consumption less than 1.8 mA and a silicon area less than 0.35 mm2.

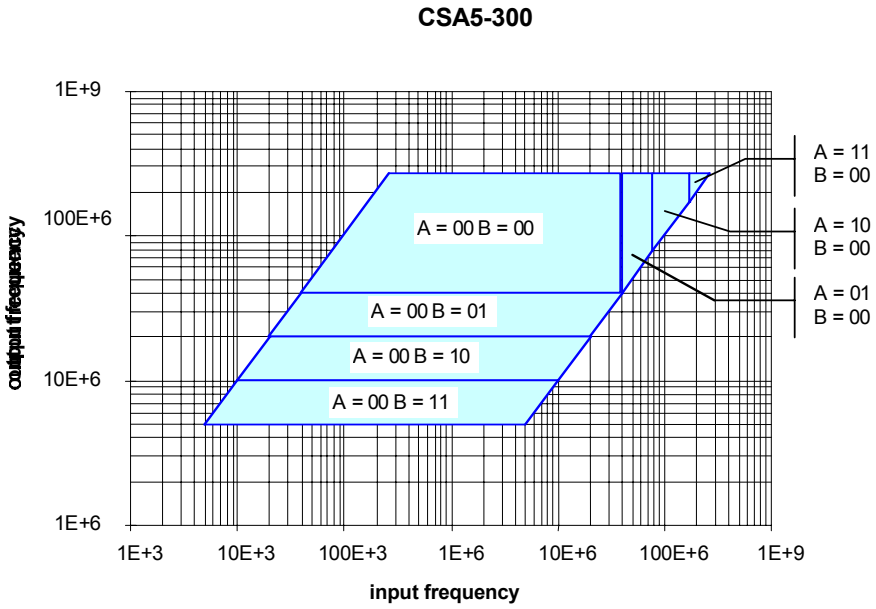
Layout - example 1

Area = 0.26 mm^2

0.35 µm

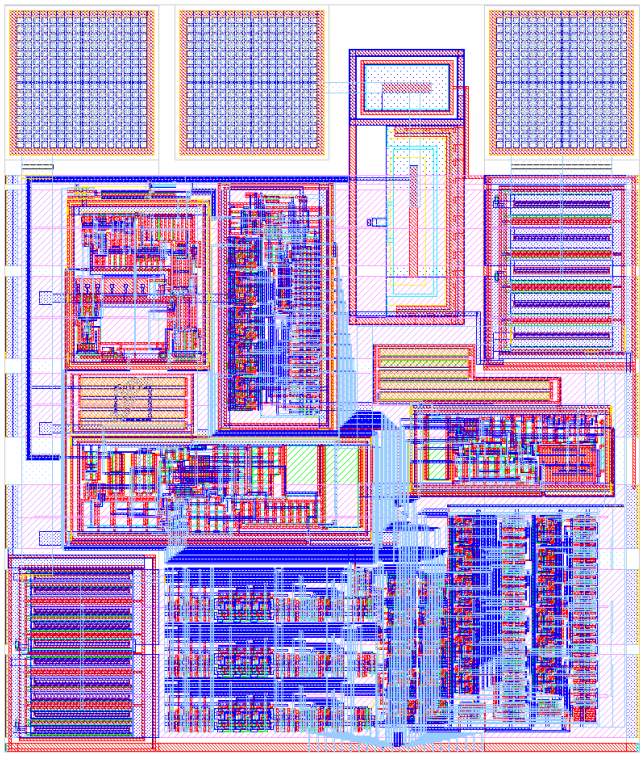


CSK applied to example 2



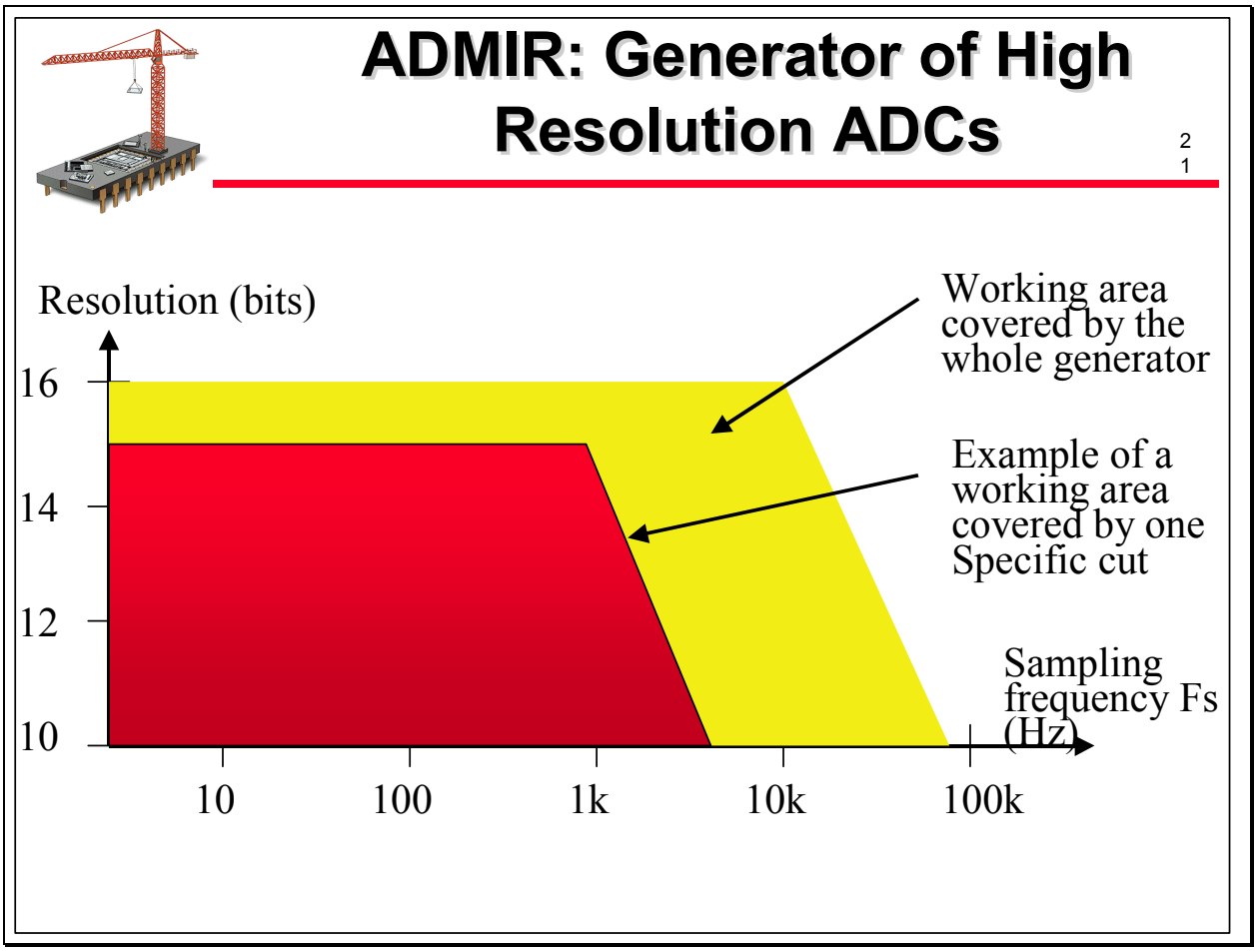
This case is different from the previous one due to the fact that the input and output frequencies may cover a wide range of values.
The consequence is that the user has to build for each application a loop divider and a loop filter corresponding to the requirements of the application. He has to follow some rules mentionned in the detailed specifications of the Virtual Component.
If we look at the slide, the VCO working area is for A and B equal to 00, meaning that the oscillating frequency is between 40 MHz and 250 MHz, The other input or output frequencies arebained thanks to an input divider or an output divider programmed by A and B.
The resulting Virtual Component is working between 1.6 V and 2.75 V in a 0.25 µm CMOS process
The typical performances reached with a 0.25 µm process is a power consumption less than 1.1 mA with an ouput frequency at 250 MHz and a silicon area less than 0.07 mm2.

Layout - example 2



Area = 0.11 mm^2

0.25 µm



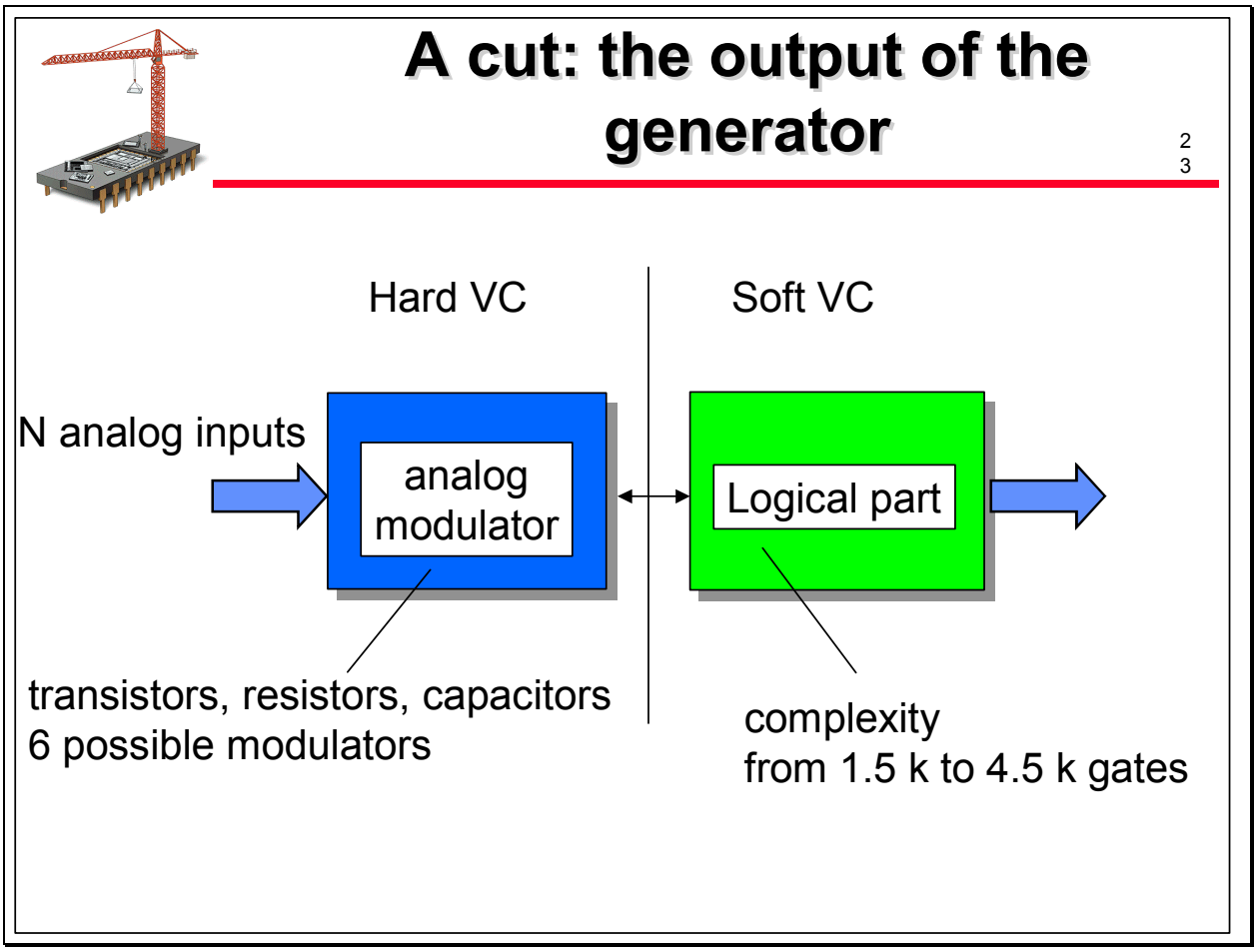
For high resolution Analog to Digital Converters, our approach is based on a generator called ADMIR.
The generator works like an embedded memory generator. The purpose is to deliver to the user a « cut » which is an Analog to digital converter with characteristics matching the described needs.
ADMIR has been designed to offer solutions for high resolution converters, between 10 and 16 bits and with sampling frequencies from DC up to 50 kHz.
This large working area has been specified to target various applications fields like data acquisition, sensor interfaces, measurement and instrumentation, power management automotive applications…
Each cut delivered by the generator is a Virtual Component. The conversion principle in ADMIR is based on an incremental converter so that each cut contains an analog part, delivered as a hardware Virtual Component, together with a logical part, delivered as a software Virtual Component.
The flexibility is obtained not only with the large working area but also with additionnal features
How does the generator work from a user 's point of vue: the generator offers a graphical user interface; the user specifies some parameters corresponding to the main characteristics of the expected resulting ADC; the parameters, mentionned on the next slide are:
- the number of analog channels: it may be chosen from 1 to 12
- For each analog channel, the user may chose between a fixed input and a programmable input.
Fixed means that the resolution and the sampling frequency of this input are fixed.
Programmable means that they can be changed by the user while the chip is operating. In such a case, the user must specify to the generators the limits of working.
- For each channel, the user may chose between a differential or single ended input

ADMIR Flexibilities

- Working area
- Number of analog input channels = between 1 and 12
- For each analog input: fixed or programmable
- For fixed inputs: #codes, INL, DNL, Fs, choice between differential / single ended,
- For programmable inputs: #codes, INL, DNL, Fs, the choice between differential and single-ended remains possible during the working mode
- The use of internal or external voltage reference
- stand-by, shut down and normal modes
- zero tuning mode for an offset-cancellation of each channel separately

Additional flexibilities are offered by the various working modes available for each cut:
- Stand by mode
- Power-down mode
- zero-tuning mode for each channel separately
- normal mode

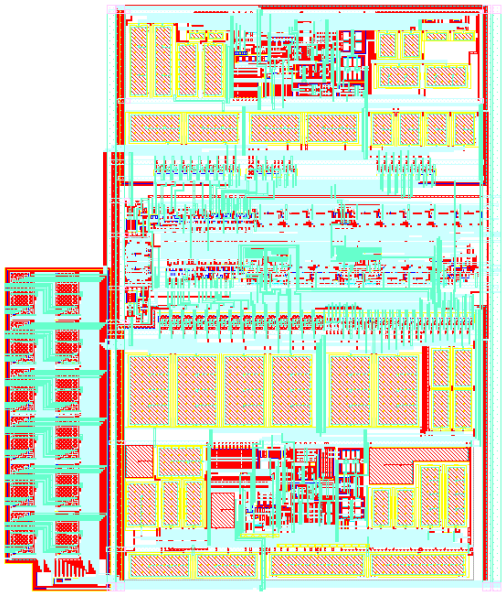
How is it possible to reach so much flexibilities:
To answer this question; I will explain briefly how the generator is built.
The generator is an algorithm written in C. This algorithm analyses the parameters given by the user and first of all analyses if the cut asked by the user may be or not generated by the generator.
The algorithm used by the generator exploits directly the results of simulations of basic cells. Indeed, there is a tight correlation between the results of simulations of some basic cells and the main characteristics of the ADC, i.e the INL and DNL.



The flexibilities are given partially by the logical part and partially by the analog part.
As an example, the logical part manages the various working modes, and in case of a programmable input, manages the programmable sequencer allowing the user to change the resolution and the sampling frequency of the concerned channel.
For the analog part, the generator choses one among six possible analog modulators. The analog modulators are 6 fixed hard macrocells, built with 14 different basic cells. The performance of the 6 analog modulators are different and allow to cover the overall working area specified in the previous slide.
When the generator concludes that the cut is possible, different views are then generated: mainly a RTL verilog model and test bench for the logic part, a GDSII file and a SPICE netlist for the analog part plus documentation, abstracts and other views.
When the basic cells have already been characterized in a specific process, it takes 2 minutes to generate the cut.
Another advantage of this generator approach is that additionnal features may be continuously added like:
- extension of the working area by increasing the number of basic cells,
- specific version for very low power or higher speed.

ADMIR applied on example 3

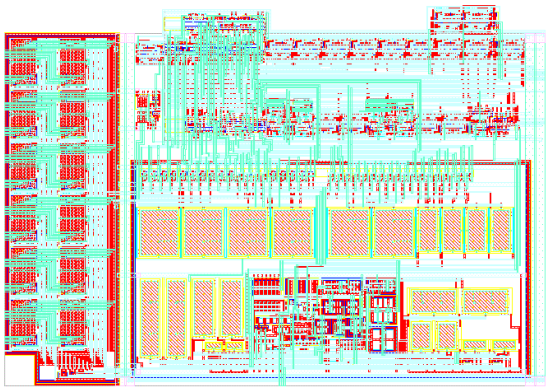
- Cut generated by ADMIR
  - Silicon area of analog part: 0.5 mm2
  - 4500 gates
  - Power consumption < 2 mA



Remember the first example of ADC for the circuti breaker. The main requirments were 11 analog inputs with some of them requiring high resolution, 13 bits DNL and INL.
The generator was able to generate the corresponding cut and you have the main characteristics described on the slide; we did not mention again the DNL and INL but give the results of the generator: a silicon area of analog part of 0.5 mm2, 4500 gates for the logic part and an overall power consumption lower then 2 mA.
All these characteristics are obtained in a pure logical 0.35 µm CMOS process. The capacitor used in the switched capacitor modulator are realized as sandwitch capacitors between polysilicon and some metal layers.
The slides gives a look at the layout of the analog part.

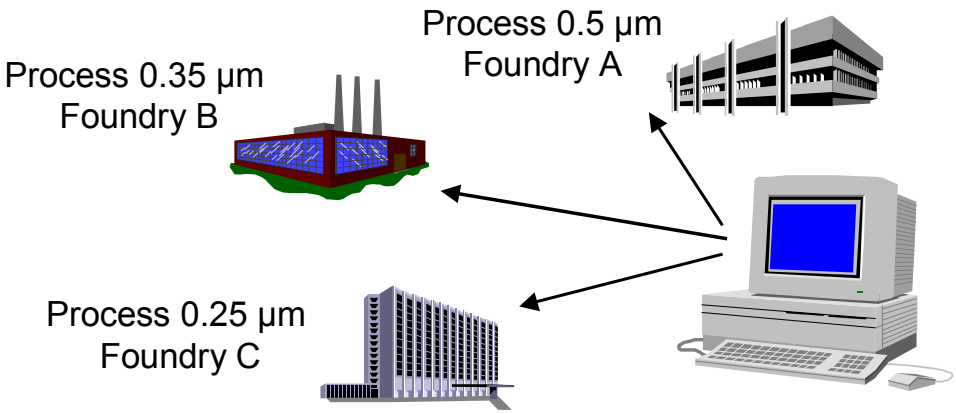
ADMIR applied on example 4

- Cut generated by ADMIR
  - Silicon area of analog part: 0.3 mm2
  - 1600 gates
  - Power consumption lower then 1.3 mA
  - INL < ± 10 E-3



The result of the generator for the second example of flexible ADC is shown on the slide. The complexity for the analog and logic parts are lower than the previous example.
This cut has also been implemented in a 0.35 µm pure logic CMOS process, the silicon are of the analog section was 0.3 mm2 and the power consumption less than 1.3 mA.

Retargetability



Retargeting = migration of schematics and layout designed with portable rules towards a targeted process

First let us define what means "retargeting": it means migrating an initial data base including schematics and layout towards a targeted process. At Dolphin, the initial data bases are designed with portable design rules.
We are speaking of horizontal portability when the original and targeted design rules belong to the same family (e.g. 0.35 µm process) and vertical portability when the original design rules and targeted design rules belong to two different families (e.g. 0.35 µm and 0.25 µm processes)

The bases for an efficient retargetability methodology

- Efficient
  - Quick
  - Secure
  - Previsibility: maintaining performances (size, speed, dynamic…)
- Retargetability of schematics
  - Portable design of hard cells
  - Hierarchic approach
  - Analog test benchs associated to each basic cell
  - Simulation models and generic parameters
- Retargetability of layout
  - Maintains topology to guarantee silicon area and performance
  - Automatic retargeting
  - Minor handcrafted modifications

A retargeting methodology will be efficient if:
- it offers quick results to satisfy TTM and cost,
- it is previsible, meaning that the performances (power consumption, speed, dynamic, silicon area and so on) can be anticipated with a high degree of confidence
- it is secure, meaning that the overall quality and reliability of the original design is maintained or increased

To achieve such goals, the retargeting process we apply at Dolphin encompasses two steps: the retargeting of the schematics and the retargeting of the layout.

The retargeting of the schematics is based on a hierarchical approach: during the original design of a complex cell, we divided it in basic cells and the overall performances of the complex cell are guaranted by the performances of the basic cells. Each basic cell is a harware cell designed using portability principles: portable schematics, analog test bench together with documentation associated to each cell, usage of extended simulation conditions and parameters.

The retargeting process uses the analog test bench and associated documentation to check that the performances of the cell are unchanged in the targeted process with specific simulation models and parameters.

The retargeting of the layout is based on the usage of portable design rules for the original design. Such portable design rules exist for each family of processes: one for 0.5 µm, one for 0.35 µm…

The principle of the layout retargeting is to apply automatic migrations to the original portable data base to obtain a data base compatible with the layout rules of the targeted process. The advantage of this methodology is that the topology is kept during the retargeting process, which is very important when we know that the performances of an analog design may highly depend on the topology. Most of the time, minor handcrafted modifications are necessary to finalize the layout.

Schematics Portability

- Top-down and bottom-up approach
  - Correlation between basic cell and overall performance
  - Independant basic cells
- Portable schematics
  - With Robust schematics, designed for ensuring the largest compatibility with any submicronic CMOS process
  - Standard BSIM3V3 Simulation models
  - Extended simulation parameters
    - Issued from experience: transistors models parameters with some extended range e.g. VT range
    - Extension of some external parameters: power supply or temperature range

Let us detail now both steps and start with the schematics
A retargeting methodology is based on two phases: the first one corresponds to the first design, for example the design of a new Analog to Digital Converter, resulting in portable schematics of this ADC and the second phase which will be the retargeting of this ADC toward a specific process.
If the design of the schematics has been thought with portability and reusability in mind, the retargeting towards a new technological process will be easier.
Several rules are used during the first phase to achieve an efficient retargeting methodology:
A- The Top-down approach
The portable schematics have to be split in independant basic cells: independant meaning that each basic cell can be simulated and characterized separately and that if the performances of the cells reach a given set of values for well defined characteristics, the performance of the whole function will be guaranted: this is an important assumption the designer has to check carefully. Indeed, it requires to make and to check a correlation between the characteristics of the basic cells and the overall characteristics of the ADC.
Typical basic cells are a VCO, an operational amplifier or an analog comparator.
This is what we call the hierarchic approach; it allows to save time on two ways during the retargeting process step:
- first, the retargeting of each basic cell can be done separatey so the retargeting of several cells may be parallelized
- secondly, it is not necessary to make simulations of the whole ADC to guarantee its performances: indeed such overall simulations would require to have retargeted competely all basic cells and to have made their assembly; potential problems of functionality or performance could be discovered very late in the retargeting step. This is not the case with our methodology.

Data Base for Portability

- Analog test bench
  - Set of simulation files
  - Set of command files
- Automatic tools for
  - Running simulations
  - Extracting characteristics
- Documention
  - Priority of simulations
  - Critical items

B - Portable schematics
This is the next rule. Designers do not use specific schematics, including a high sensitivity to some parameters like the power supply voltage, the temperature, the parasitics capacitors … or do not use some specific feature of a given process:
This is maybe where there is a real know how making the difference between poor, good and excellent analog designers or between beginners and experienced designers. Without revealing secrets, let us say that rules like the following have to be respected:
- do not use specific devices of a specific process like high voltage transistors, floating diods or resistors with high resistive values
- do not use absolute values but only ratios (resistors and capacitors)
- use current mirrors to generate multiple or sub-multiple of currents
- do not use too much cascoded transistors
- use multitage (3, 4) operational amplifiers
- use differential structures to increase noise immunity
- use separate voltage for analog and logic circuitries

C- Analog test bench and associated documentation
Saving time during a retargeting process phase requires finding potential problems as earlier as possible. That is the reason why the first design has to be documented and the critical point of each cell has to be described.
What contains such a documentation:
First, what we call an analog test bench: an analog test bench is a set of files necessary and sufficient to functionnly validate and characterize the analog cells.

Analog test bench Parametrized SPICE Netlist


```
…
PS= 16.2U  PD= 16.2U
.ENDS PFD
// ---------------------------------------- TEST_PFD ---
//    Analog top-level description:
// ---------------------------------------------------------
>>> SPICE
  XI1       A0 A1 A2 A3 CKNEG CKPOS DDOWN DUP EFIL POLN SB DOWN UP LOCK
OUT PFD
  R1        N1 NR1 '2000*COEFRNM' TC=4.3E-3,14E-6

.param alim={VA}
.param COEFRNM={COEFRNM}
.param COEFPOL={COEFPOL}
.param alim2=1.5
.param alimrefp=1
.param adiff=0

VDD VDD 0 alim
VSS VSS 0 0
IPOLC 0 IPOLC '10e-6*COEFPOL '
…
```

What we find typically in such files are the SPICE netlist of the basic cells; typically including parameters like resitors and capacitors, for example output loads of an operationnal amplifier. In this file the technological case (worst case, typical case, best case) corresponding to the parameters of the devices models is also described.
An example of the subset of a SPICE netlist is shown on the slide; this one includes parameters like power supply voltage (VA), a coefficient (COEFRNM) for the variation of the resistor value to cover the range specified in the electrical rules of the targeted process, a coefficient (COEFPOL) for the variation of the current of a polarisation cell to cover the range given by the result of another simulation.
Together with the SPICE netlist, a command file for the simulation contains the description of all signals to be applied to the cell; this command file may also contain parameters like signal frequency and amplitude.
A third file fixes the values of each parameter specified in the previous file; this file is used by a tool, called « Shaker », developed by Dolphin to run automatically the various simulations with different values of the parameters and extract, in each output simulation file, the values of the characteristics required by the designer. On this way, the analog designer can be focused on the analyse of the results and do not spend time to prepare and analyse the results of the simulations.
An example of such a file, with a very simple syntax is given on the next slide.
Indeed to completely validate and characterize an operationnal amplifier used in the design of a high resolution converter, typically 600 « simulations » are necessary. We easily understand that without a minimum of documentation and automatic simulations and characteristics extractions, such a work could quickly become a nightmare!

Schematics Retargeting
Example of a « shaker » file - 1


```
********** shaker file ********************************
*********************************************************************
.SIMULATION 01
DEFAULT 2
FROMREF test_pfd TOSIMUL ff020 OPTION TRAN
TITLE simulation fast
PARAMETER
VA = 1.6
COEFRNM = 1.2
TEMP = -40
COEFPOL = 0.92

.SIMULATION 02
DEFAULT 2
FROMREF test_pfd TOSIMUL ff022 OPTION TRAN
TITLE simulation fast
PARAMETER
VA = 1.6
COEFRNM = 1.2
TEMP = 125
COEFPOL = 0.65
……
```

The documentation must also contain an order of priority of the simulations. At this step, the order of priority concerns the basic cells. To illustrate, let us come back on the operationnal amplifier designed for a high resolution ADC; if the critical characteristic of this ADC is the INL, the cell to be simulated first is the opearationnal amplifier used in the first stage of the ADC. The characteristic to check first for this operationnal amplifier is the settling time and the worst case for this characteristics occurs when the output load is maximum, the power supply voltage and the temperature maximum and the transistors operating in worst case of process. But the worst case may depend on the characteristics of the targeted process. This worst case will be identified later, at the beginning of the retargeting step.
On this way, during the retargeting process, if the results of this first simulation are acceptable, the chance to have no modifications in the design are strong ; if the results are not acceptable, the designer can analyse the more critical issues very early in the retargeting process step.

D- Models and parameters of devices

To be sure that the design will have the required performances in various process, two methods have been historically applied in our Company:

- The use of generic parameters: starting from a set of parameters representing different processes, the analog designer fix himself a set of parameters corresponding to an enlargment of the parameter values range; this operation is done for the main parameters like the threshold voltage, oxyde thickness, carriers mobility…
- To take a significant margin on some other simulation parameters like the power supply voltage and the temperature.

All the art of the analog designer will be to fix the minimum and maximum values to apply to be enough portable.

Schematics Retargeting
Example of a « shaker » file - 2


```
.EXTRACTION

GAIN = Gout  NODE = VDB(OUT)
 FREQREF = 10

FREQUENCE = GBout NODE =  VDB(OUT)
 GAINREF = 0

PHASIS = PHIout  NODE =  VP(OUT)
 NODEREF =  VDB(OUT) GAINREF = 0

INTEGR = conso NODE = I(EOUT)
AFTER = 1255n
BEFORE = 1305n
.RESULTS

Ivdd_1 = conso_1 / 1.205e-6
Ivdd_2 = conso_2 / 1.205e-6

.DATASHEET
Simul;VDD;COEFRNM;Temp;Ivdd moyenne sur 360
ff020;{VA_1};{COEFRNM_1};{TEMP_1};{Ivdd_1}
```

The tendancy is now to apply the second method which presents mainly two advantages compared to the first one: the first one isto know the margin of the design regarding a fundamental parameter like the power supply voltage and the second one, more pragmatic: parameters like power supply voltage and temperature are more easy to manipulate than thetransistors models parameters.

E- Documentation for the critical parts of the schematics

Last but not least. Every analog designer designing accurate functions knows that there are often critical devices inside a cell: there are several kinds of criticity: for example transistors requiring a rigorous matching between them for reducing the potential offset; but a schematic may require some tuning for an optimum performance, for example in power consumption or speed, by the modificafion of some transistors dimensions: in both case, the designer will mention it in the documentations.

Some hours will be saved during the retargeting process.

That ’s all for the first step which is the initial design. The overall methodology may appear quite complex but we observe a similar effect than in the design of an embedded memory generator: Indeed, if you have to design one memory instance, for example a 128 k bytes, you do not need to design a generator. But if you intend to generate a lot of instances in various designs, with various characteristics, it is better to design, or to buy a generator. It is an investment with its own ROI! The issue is the same in analog design.

We can now discuss of the retargeting step itself.

Example of documentation

…
This directory is used to simulate the Phase and Frequency Detector.
It is used to determine the characteristic I.dt=F(Phase)

The steps of the method are the followings:

1. Take care to the ADVISES above.
2. In the 'comphase' schemsim directory on PC, generate your 'comphase.nsx' netlist file from the SCS Hierarchy.
3. Run 'SHAKER comphase -c' on UNIX.
4. Run 'SHAKER comphase -e' on UNIX.
5. Run 'SHAKER comphase -r' on UNIX.
6. Transfer the 'comphase.dst' results file on PC in the 'comphase.xls' file.

ADVISES:
1. Be sure the biasing coef 'coeffpol' have been updated to the targeted technology process.
2. The worst cases are ss000, fs000, sf000, ff000 (low VDD=1.8V and high coeffpol>1).
   You must take care to the following points:
 2.1 POLP must not be too low (under VDSsat of M2, M3, M4, M5 and M32), else an error of current copy may occur. If it is the case, you may increase
     the width of M17 (and the attached transistors).
…

F- Retargeting of the schematics

A new customer now requires the retargeting of our ADC into a new process. How do we proceed?

The purpose of the retargeting step of the schematic is to obtain as quicker as possible a new data base of schematics with the right performances in the new process. Our retargeting methodology follows similar principles applied for the industrial test of Integrated Circuits: to save time, most critical tests patterns (here simulations) are done first. On this way, the probability to have bad surprises during the retargeting process is decreasing drastically when the retargeting step progresses.

Portable schematics are available. It means that all the previous described work has been done and that to each basic cell are associated a set of files (simulation, command, parameters) and a set of documentation.

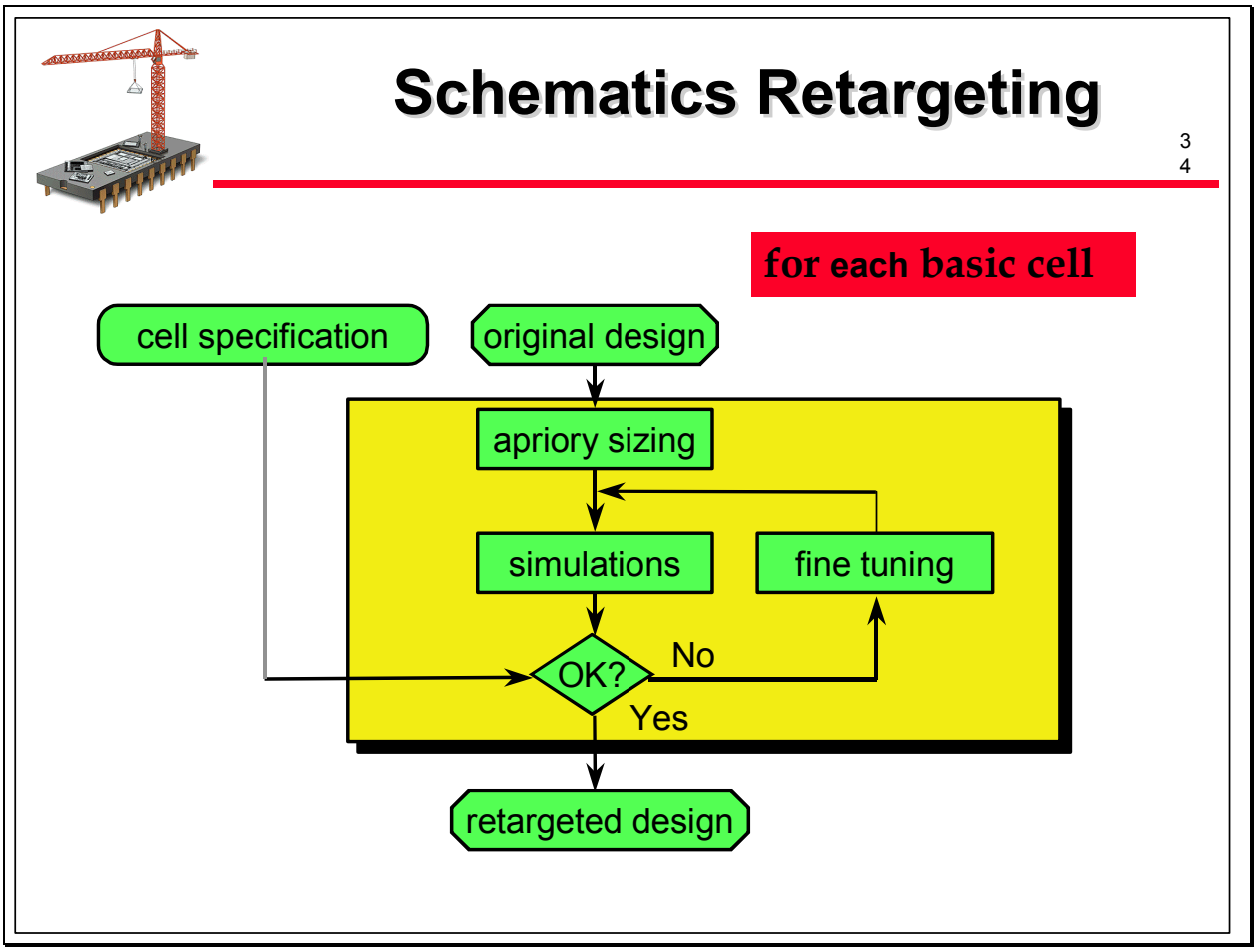
First we need to have access to the design rules, including electrical parameters of the targeted technological process and transistors models in a standard format like BSIM3V3.

The retargeting process will itself contain several steps:

1- Analyse of the main electrical features of the process

This analyse is done by running electrical simulations on single devices; typically curves like IDS = F(VDS) parametrized with VGS are obtained and analysed by an experienced designer.

The purpose of this analyse is to determine what are the critical items of the process. The result of this analyse is to complete the definition of priority for the simulations of each basic cell which was pre-established.



2- A-priori sizing of the transistors
Basic cells are classified in two categories: the first category are cells which can be shrinked to benefit of the advantages of the targeted process: this is typically the case of phases generators where transistors with minimum length are use, or for most of the time for the basic cells of a PLL. The second category are cells containing critical transistors: for this cells, two steps are applied for the retargeting: a general shrink and size on all transistors of the cell followed by an a-priori tuning of some transistors dimensions. The shrink ratio may be different for the two catagories of cells.
Such a job is realized by an experimented designer with the help of all documentation previously discussed.
The result of this a-priori step is a new schematic data-base, ready to be simulated.
3- Simulations
For each cell, the simulations are then run, using the real transistors models and associated parameters corresponding to the targeted process. The pre-defined priority of the simulation is respected and the characteristics automatically extracted.
Two cases: if the targeted characteristics are met, the retargeting continues,
if some characteristic is not met, once again two cases: the analyse of the simulation result shows that a simple modification of transistors dimension may be done: it is generally the case if the portable design has followed the rules previously described. For the other cases, extremely rare, there are two possibilities: the impact on the overall performance are acceptable in the application of the customer and the specifications are modified. If the impact is not acceptable, a deeper modification of the cell has to be done. Until now, we have never been in this situation.

Main characterisitics of the method

- Systematic and rigorous
- Parallelization
- Concentration of designers on critical issues
- Pre-existing data base for new performances
- Pre-existing data base for new cells

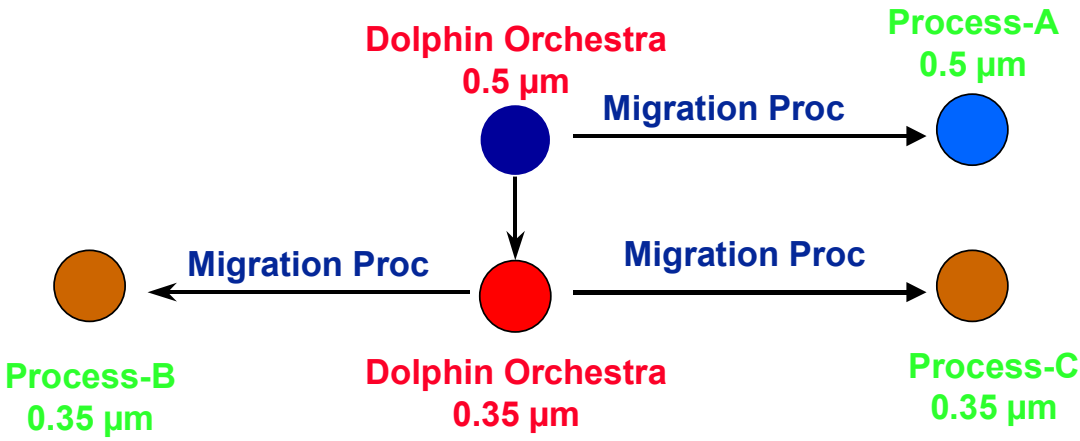
The advantages of this method are multifold:
- To be systematic and rigorous
- It can be applied by analog designers who do not have a deep knowledge of the cell they are simulating; it represents also an excellent training job for young analog designers
- It allows experienced designers to focus on difficulties, if any, or to innovative solutions for new designs, or to modifications of characteristics required by the customer
- It can be parallellized for each basic cell

4- Case of modifications required by the customer application
Modifications may be the requirement for a new functionality or for the same functionality but with different performances, like dynamic characteristics or power consumption for example. In both cases, all the accumulated data base is used .
New functionnality often require new basic cells but new basic cells are often built from previous ones. Existing documentation and simulations files allow to speed-up the process of designing new cells and to have a better confidence in the result.
New performances require that the work of correlation between performance of an overall function and its basic cells has been done. In this case, it will be quickly decided if the new performances require the design of a new basic cell or if modifications of the existing one are enough. Here again, the existing documentation and simuations are helpful.

Dolphin Orchestra Portable Rules

Mix of **vertical** and **horizontal** retargeting

- vertical retargeting uses shrinking and sizing
- horizontal retargeting uses sizing



LAYOUT RETARGETABILITY

The layout retargeting methodology is also based on two steps: the first step corresponds to the first layout of a function, realized using portable design rules and the second step which will be the retargeting towards a specific technological process of a specific manufacturer. Here again, if the design of the schematics has been thought with portability and reusability in mind, the retargeting towards a new technological process will be easier.

Let us look at the first step, the design using portable design rules.

A- Portable design rules

Dolphin have been using portable design rules, called Orchestra, since a lot of years. A set of portable design rules is established for each family of process. So Orchestra design rules exist for the 0.5 µm family, 0.35 µm family and so on.

We speak of vertical retargeting when the retargeting is done between two different families like 0.5 µm and 0.35 µm or 0.35 µm and 0.25 µm; we speak of horizontal retargeting when it is done in the same family, for example the retargeting from the 0.5 µm portable design rules towards the 0.5 µm design rules of a specific foundry.

Each set of portable design rules is established after examination of several sets (minimum 3) of specific design rules coming from different foundries or semiconductors manufacturers. These design rules are not systematically based on worst cases values, which would have significant consequences on densisty but on analyse of critical layout paths. This analyse is done with an excel speadsheet.

Portable Layout Rules

	Dolphin035	MAXI035	F1	F2	F3	F4	F5
Desox	1,400	1,400	1,100	0,900	1,100	1,340	1,000
Poly1	0,950	1,060	0,800	0,800	1,000	0,820	0,800
Contact	v	1,000	0,900	0,800	0,900	1,000	0,800
Metal1	v	1,280	0,950	0,950	1,000	1,200	0,900
Contact desox	1,700	1,780	1,500	1,300	1,600	1,640	1,300
Contact poly	1,600	1,660	1,150	1,150	1,300	1,420	1,150
Contact Metal1	1,700	1,560	1,150	1,150	1,200	1,480	1,150
DiffN DiffP	3,400	3,480	3,300	3,100	3,400	3,400	2,900
DifN DifP avec mindx	3,100	3,100	2,900	2,700	2,900	3,100	2,600
p1 entre 2 diff	1,550	1,560	1,050	1,050	1,500	1,080	0,650
mos P min	2,550	2,720	2,250	2,050	2,500	2,560	2,050
mos N min	v	2,720	2,250	2,050	2,500	2,560	2,050
Bout de Mos avec P1	1,700	1,810	1,400	1,350	1,700	1,480	1,350
Bout de Mos avec DX	1,450	1,530	1,100	1,150	1,400	1,240	0,950
via	1,250	1,220	0,900	0,900	1,000	1,220	0,900
Metal2	1,400	1,400	1,050	1,000	1,100	1,400	1,000
Pas routage M1	v	1,440	1,125	1,125	1,250	1,360	1,050
Pas routage M2	v	1,500	1,150	1,125	1,200	1,500	1,125
Pas routage M3	1,500	1,600	1,150	1,125	1,300	1,500	1,125
LDIF pour simul	1,100	1,180	0,950	0,850	1,100	1,100	0,850
W min	v	1,080	0,900	0,700	1,000	1,000	0,700

For a new family, a first version of the portable design rules is built, typically with a shrink of the previous family. Then, for each targeted process, we examine the shrink ratio which has to be applied to a portable layout to generate automatically a targeted layout. Ideally, such a ratio should be equal to 1 for processes in the same family and equal to the ratio of the minimum transistors gate lengths between two families; for example 0.7 between 0.5 µm and 0.35 µm families.
If such a ratio is homogeneous for the different targeted processes, the portable rules are fine. If this ratio is not homogeneous, we modify the rules to make it more homogeneous.
The portable design rules are the results of this analyse.
Some elementary guidelines are also included in portable design rules:
- not use devices specific of some processes, already mentioned for the portable schematics
- use only angles multiple of 90°
- apply the worst case for specific rules like large metallisation connections, antenna rules, latch-up…

The slide shows the differences between worst case approach and analyse of critical layout path. The lines represent critical layout path, for example routing pitch of metal one, metal 2, poly…. The rows represent the values obained for these critical layout paths for the Dolphin portable rules, layout rules based on a worst case principle and the targeted processes from different manufacturers. Some values have been cancelled for confidentiality reasons. As an example of critical layout path is the Metal3 pitch which is the sum of half the width of metal3 lines, the distance between two metal3 connections, half the width of a via2 and the oversize of metal3 with reference to via2.
The table shows that for portable rules, the obtained value is lower than the value for the worst case.

Example of subset of Verification Files

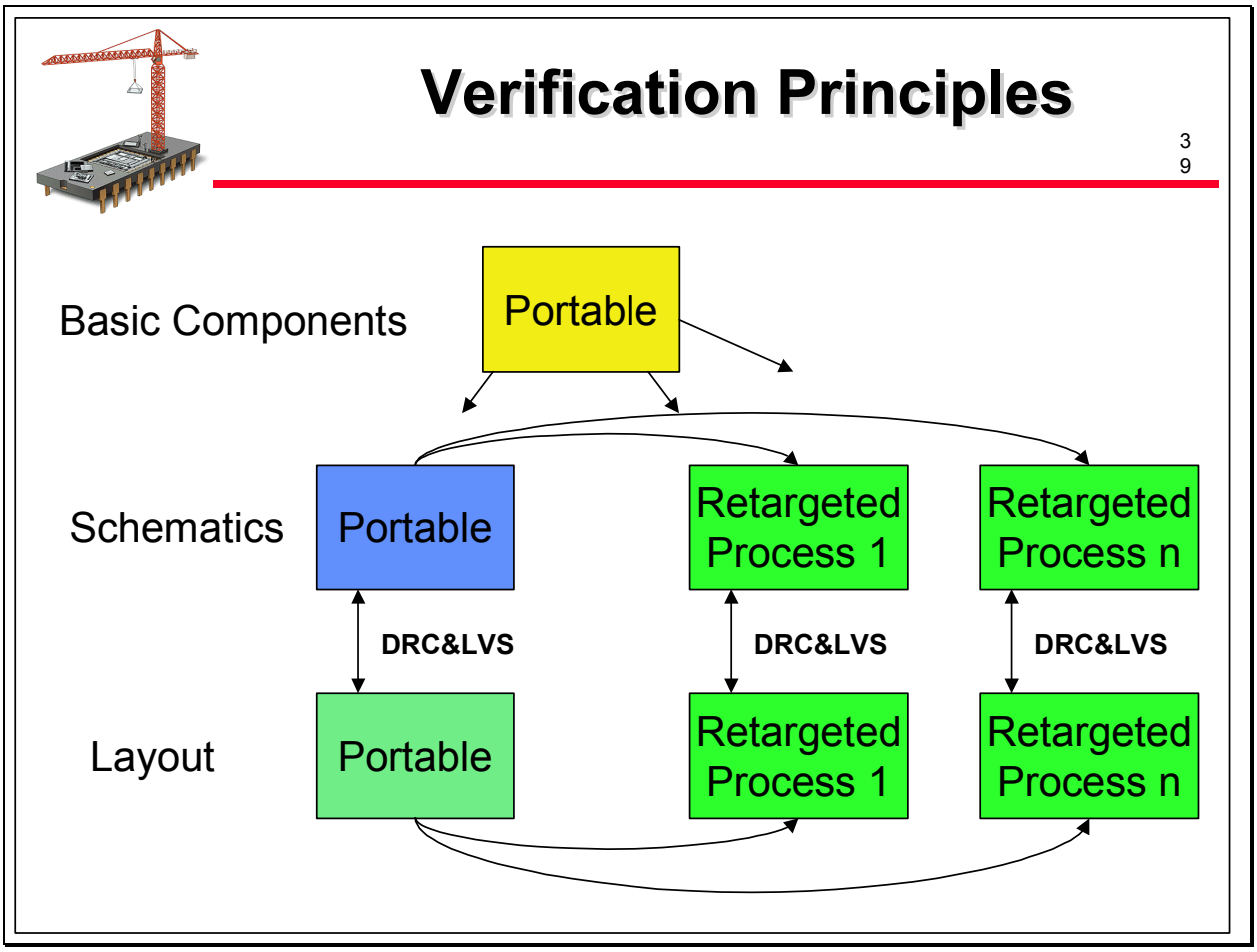
Example of subset of the file describing the DRC configurations

```
…
(W_LMET1      = tGeParam (tf "W_LMET1") )      ;Rule E1
(S_LMET1      = tGeParam ( tf "S_LMET1") )     ;Rule E2
(S_LMET1_VM1XL = tGeParam( tf "S_LMET1_VM1XL") ) ;Rule E2_xxl
(S_VM1XL_VM1XL = tGeParam ( tf "S_VM1XL_VM1XL") ) ;Rule E2_xxl
…
```

Example of subset of the file describing the values to be applied for DRC in portable design rules

```
…
(W_LMET1        0.60) ;Rule E1
(S_LMET1        0.70) ;Rule E2
(S_LMET1_VM1XL          0.70) ;Rule E2_xxl
(S_VM1XL_VM1XL          0.70) ;Rule E2_xxl
…
```

Together with this portable design rules, we have set-up a verification system for DRC and LVS based on the usage of parameters. This verification methodology uses the standard verification tool from Cadence but could be adapted to other verification tools.
The principle of usage of parameters is simple: the DRC configuration file includes all the configurations of verification with a parameter for each configuration: for example, the parameter W_LMET1 is introduced for the verification of the minimum width of the metal 1 layer. An example of the content of this configuration file is given on the slide.
Together with this configuration file, a set of technological files are described, each of them containing the value for each of the parameters existing in the configuration file. A technological file exists for the portable design rules but also for each targeted specific process. An example of the content of this file containing values is also given on the slide.
When a DRC is run, we mention to the tool the name of the technological file which has to be applied.



This methodology for portable design rules and powerfull verification system allows to save a lot of time on several ways:
- Design rules coming from manufacturers have not always the same level of maturity. For example we have seen some 0.5 µm design rules officialy released by the manufacturer without antenna rules, such antenna rules being introduced 1 year later. The simultaneous access to several design rules allows us to anticipate such situations, avoiding time consuming redesign tasks.
- Using a unique configuration file with parameters instead of values saves a lot of time and offers a better security in case of updates of the configurations description; it also avoids to create and check a new file for each new technological process.
As we can see on the slide, DRC and LVS are applied on various data bases, on portable data bases and also on retargeted daat bases. The usage of common files save time and avoids errors, is more secure and effcient than multiple verification files.

Layout Retargeting

PAS		Dolphin 0,35	F1 0,25	shrink	
	Desox	1,400	0,700	*0,5000*	auto
	Poly1	0,950	0,600	*0,6316*	auto
	Contact	1,050	0,600	*0,5714*	auto
	Metal1	1,300	0,640	*0,4923*	auto
	Contact desox	1,700	0,980	*0,5765*	auto
	Contact poly	v	v	*valeur*	auto
	Contact Metal1	v	v	*#VALEUR!*	auto
	DiffN DiffP	v	v	*#VALEUR!*	auto
	DifN DifP avec mindx	v	v	*#VALEUR!*	auto
	Poly1 entre 2 diff	v	v	*#VALEUR!*	auto
	Mos P min	v	v	*#VALEUR!*	auto
	Mos N min	v	v	*#VALEUR!*	auto
	Bout de Mos avec P1	v	v	*#VALEUR!*	auto
	Bout de Mos avec DX	v	v	*#VALEUR!*	auto
	Via	v	v	*#VALEUR!*	auto
	Metal2	v	v	*#VALEUR!*	auto
	Pas routage M1	v	v	*#VALEUR!*	auto
	Pas routage M2	v	v	*#VALEUR!*	auto
	Via2	v	v	*#VALEUR!*	auto
	Metal3	v	v	*#VALEUR!*	auto
	Pas routage M3	v	v	*#VALEUR!*	auto

-TABLEAU PORTAGE -
Révision C du : 3/09/99
par : DCA

Shrink linéaire =

calculée	retenue
####	**0,6857**

auto ou valeur **>** **0,6857**

Shrink surfacique =

####	**0,4702**

< supprimer **auto**
< pour ne pas tenir compte
< la chaine critique concernée

	Captif	Natif	Porté
Pas grille	**0,01**	**0,01**	**0,01**
LDIF	**1,10**	**0,68**	**0,75**
W min	**1,00**	**0,58**	**0,69**

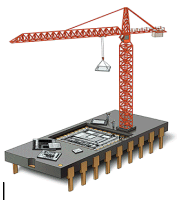
Entrer **auto** dans les cases grisées pour laisser le calcul automatique, **sinon** entrer la **valeur forcée**

B- Layout Retargeting

In the same spreadsheet we spoke about for the generation of portable design rules, are given the sizing and skrink operations which have to be done for the generation of each mask level corresponding to the targeted design rules.

See the slide for a look at a subset of this spreadsheet. Two subsets of layout rules are shown: 0.35 µm Dolphin portable layout rules and 0.25 µm layout rules coming from a foundry called F1. Some values have been cancelled for confidentiality reasons.

The spreadsheet computes automatically the best shrink ratio between the two sets of design rules.



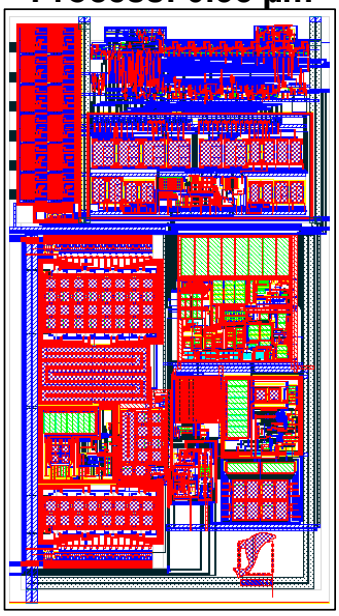
Layout retargeting

Ref	Mnemo	Dolphin035 RevC	F1 025	valeur shrinkée	migration par bord	Côtes finales	Delta		
	NWELL = LNTUB - ACTIVE = LTHOX								
A1	W_LNTUB	**v**	**v**	#VALEUR!	0,000	#####	####	####	#####
A2	S_LNTUB_equip	**v**	**v**	#VALEUR!	**0,000**	#####	####		#####
A3	S_LNTUB	**v**	**v**	#VALEUR!		#####	####	####	#####
A4	E_LNTUB_LPDIF	**v**	**v**	#VALEUR!		#####	####	####	#####
A5	E_LNTUB_LPTIE	**v**	**v**	#VALEUR!		#####	####	####	#####
A6	S_LNTUB_LNDIF	**v**	**v**	#VALEUR!		#####	####	####	#####
A7	S_LNTUB_LPTIE	**v**	**v**	#VALEUR!		#####	####		#####
A8	W_LTHOX	**v**	**v**	#VALEUR!	0,000	#####	####	####	#####
A9	S_LTHOX	**v**	**v**	#VALEUR!	**0,000**	#####	####	####	#####
A10	S_LNDIF_LPTIE	**v**	**v**	#VALEUR!		#####	####		#####
	POLY1 = LPOL1								
B1	W_LPOL1	**0,350**	**0,240**	0,240	0,000	**0,240**	0,000	0,00	-
B2	S_LPOL1	***0,600***	**0,360**	0,411	**auto**	**0,411**	0,051	0,03	-
B3	W_LPOL1_ngate	**0,350**	**0,240**	0,240	0,000	**0,240**	0,000		-
B4	W_LPOL1_pgate	**0,350**	**0,240**	0,240	0,000	**0,240**	0,000		-
B5	E_LPOL1_LTHOX	**0,450**	**0,300**	0,309	**auto**	**0,309**	0,009		-
B6	E_LTHOX_LPOL1	**0,650**	**0,300**	0,446		**0,446**	0,146		-
B7	S_LPOL1_LTHOX	**0,300**	**0,140**	0,206		**0,206**	0,066		-
B9	W_LTHOX_Wgate			0,000		**0,000**	0,000		-
	CONTACT = LCONT								
C1	W_LCONT	**0,400**	**0,300**	0,274	-0,013	**0,300**	0,000		-
C2	S_LCONT	***0,650***	**0,300**	0,446	**auto**	**0,420**	0,120		-

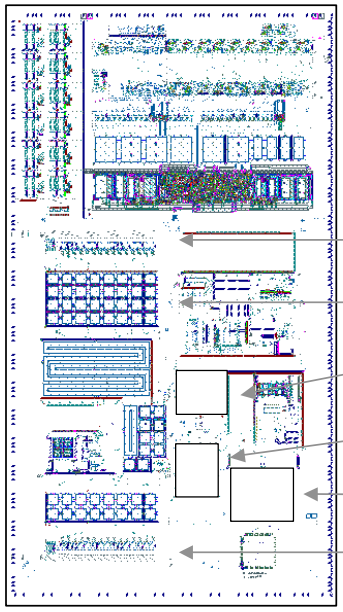
The following slide shows another part of the same spreadsheet, the sizing to be done on each mask layer is automatically computed. For example, we can see that for the first level of polysilicon layer, a single shrink operation is done and for the contact layer, the same shrink operation is done but has to be followed by a sizing of -0.013 µm on each side.
All these operations of skrink and size are done by an automatic tool and the use of such a spreadsheet guarantees that the results of the retargeting procedures will be compatible with the targeted design rules.
The layout retargeting of a complete function is done hierarchically. It means that the retargeting procedures are applied simultaneously to basic cells and to the cells containing the connexions between the basic cells. Then, all the cells are merged together by an tool to obtain the final data base of the complete function.
This methodology allows also to introduce modifications in basic cells if such modifications are necessary after the retargeting of schematics for example.

ADMIR - Example of Retargeting

Process: 0.35 µm



Difference with 0.5 µm process



Same area: 0.73 mm²

Phase generator
Capacitors
OAP1
Decoder
Capacitors
Decoder

To illustrate what has been said on the retargeting methodology test circuits of the generator ADMIR has been succesfully fabricated for three technological processes, one 0.5 µm process and two 0.35 µm processes.
These processes are pure logical processes and do not require any specific analog features like second layer of polyslicon or specific resistor layer.
The retargeting of the schematics required two adaptions starting from the portable schematics:
- some transistors sizes inside an operationnal amplifier had to be adjusted to have a better stability
- the layers used for the capacitors used in the switched capacitors integrators had to be changed due to the difference in oxyde thickness of the various processes.
The layout retargeting has been done as previously described. It had been decided to have an overall shrink ratio of one, even if some transistors inside some cells have been retargeted to have a minimum gate length corresponding to the targeted process.
You can see on the slide the difference between a dat base in 0.5 µm and the same data base retargeted in 0.35 µm process. The topology remains the same, the size of the elements and design rules only have been changed.
The only manual layout tasks were the consequences of the modifications of the schematics. There were implemented without problems, because such possibilities of tuning had been previously documented and some silicon area margin had been reserved in the portable layout..

ADMIR - Results

- Silicon Area of analog part
  - From 0.3 mm2 to 0.8 mm2 without Voltage Reference
  - Add 0.4 mm2 for the Voltage Reference
- Power Consumption
  - From 1.5 mA to 5.5 mA
- Complexity of logic part
  - From 1500 to 4500 gates
- Retargeting delay of a cut in a new process
  - Typically 7 weeks

The characterisation results on silicon correspond to specifications. The chips have good performances even outside the power supply voltage range. It means that the generator is portable towards 0.25 µm processes without difficulties.
The slide gives different results corresponding to:
- the silicon area range of the different possible cuts: note that it corresponds to the analog part only without the voltage reference. Add typically 0.4 mm2 for a voltage reference
- the complexity range of the logic part: this complexity depends on the number of channels and of the resolution required for each channel
- The power consumption range depending on all the performances
- a typical retargeting delay range for a cut in a new process

CONCLUSION

- Infinite number of technical requirements
  - -> Flexible solutions required
- Demonstration of existing solutions
  - -> PLLs and high resolution ADCs
- Future trends
  - -> other functions : DACs, Codecs…
  - -> retargeting enhancements
  - -> addition of testability

During this presentation, we have successively shown that the design of Analog and Mixed Signal Virtual Component is highly demanding for the delivery of various functionalities, performances, in multiple processes, which are the common life of SoC design.
This demand makes impossible to propose a catalogue of fixed products; the solution proposed by Dolphin and illustrated through two families of AMS VCs , PLLs and high resolution ADCs, is to offer an approach based on kits and generators allowing the generation of solutions matching 100% of the application requirements with a high level of security ; a strong retargeting methodology, also described in this presentation is an essential issue.
This methodology has been applied by the Company since several years and is permanently evolving.
Future evolutions are expected in various areas like:
- the extension of the kit and generators approach to other families of AMS VCs like DACs, codecs…
- the optimization of schematics when migrating from a process generation to the next one with a change of power supply voltage
- the layout compaction while keeping some topology constraints for maintaining performances, quality and reliability
- the inclusion of testability methodology, another bottleneck of mixed signal design
- …