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Sigma-Delta Converters for Multimedia Applications

Axel Alegre de La Sougeole, Christian Perrin
SGS Thomson
Jean-Francois Pollet
Dolphin Integration

314M

SIGMA-DELTA CONVERTERS FOR MULTIMEDIA APPLICATIONS

Axel Alegre de La SOUGEOLE - SGS-THOMSON
Christian PERRIN - SGS THOMSON
Jean-François POLLET - DOLPHIN INTEGRATION

SGS-ThOMSON
2055 GATEWAY Place, SUITE 300
SAN JOSE, CA. 95110
Ph. (408) 452 - 8585
Fax (408) 452 - 1549

DOLPHIN INTEGRATION
8, chemin des Clos - ZIRST
38 242 MEYLAN - FRANCE
Ph. (33) 7641 1096
Fax (33) 76 90 29 65

INTRODUCTION

This paper mainly presents macrocells for the design of delta-sigma converters, available in the ASIC library of the SGS-THOMSON BICMOS 1.2 gm technological process.

These macrocells can be used to build ASICs containing stereo analog-to-digital and digital-to-analog converters for multimedia audio applications.

In a first part, macrocell characteristics and a "kit part" circuit are presented.

In the second part, the methodology for specifying essential characteristics of delta-sigma converters is illustrated through the use of a programable delta-sigma analog-to-digital converter circuit In the third part, a brief description of other available cells in the same library is given.

In the fourth part, future developments in the same domain are shortly described.

1- DELTA-SIGMA CONVERTERS MACROCELLS FOR MULTIMEDIA AUDIO APPLICATIONS

1-1 ARCHITECTURE

a) Delta-sigma conversion

Our purpose here is not to explain in detail the delta-sigma conversion principles but to roughly describe the architecture of such converters (see figures 1 and 2).

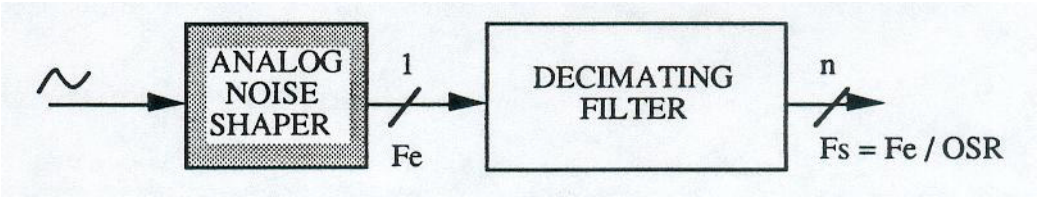

Figure 1 - ΔΣ Analog to Digital Converter

A delta-sigma analog-to-digital converter is comprized of an analog front-end followed by a digital decimating filter. The analog front-end, often called modulator or "noise shaper" oversamples the analog signal ("over" compared to the bandwidth of the signal to be converted, typically some MHz) and delivers to the digital filter a serial one-bit stream at high frequency. The purpose of this analog part is to reject out of the signal band the quantization noise by applying to this noise a high pass filter; the remaining noise in the band then corresponds to that of a high resolution A/D converter but with a high frequency one-bit data output. The purpose of the decimating filter then is to filter the out-of-band noise and to increase the number of bit (typically from 1 to 16) while decreasing the sampling frequency.

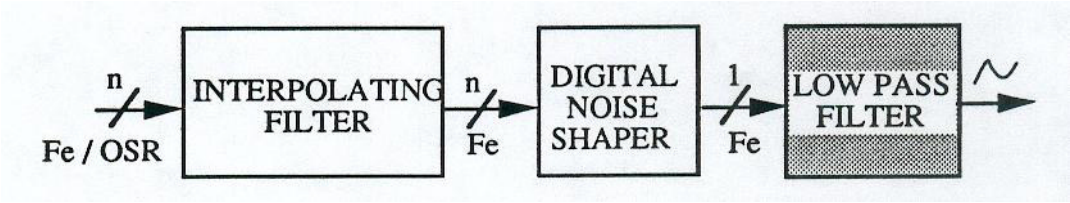

Figure 2 - $\Delta\sum$ Digital to Analog Converter

Dually, a delta-sigma digital-to-analog converter is comprized of a digital front-end followed by an analog part. The purpose of the digital front-end is to generate a high frequency digital one-bit stream which contains the signal and the quantization noise. The digital part is comprized of an interpolating filter and a noise shaper; the filter attenuates the signal images due to the interpolating operation; the noise shaper has the same role as the analog part in an ADC. The analog part has to convert the digital one-bit stream to an analog signal while filtering the out of band noise.

Numerous architectures and implementations exist for noise shapers (analog and digital) and for such filters, due to the various performances aimed-at and on the technological processes targetted.

b) Macrocells of the library

In the case of the BICMOS 1.2 .tm library, four macrocells have been designed and made available: two for the AD Converters and two for the DA Converters.

- a stereo analog delta-sigma modulator (cell 1 for the ADC)
- a stereo digital decimating filter (cell 2 for the ADC)
- a stereo digital interpolating filter and a stereo digital delta-sigma modulator (cell 3 for the DAC)
- a stereo analog low-pass filter (cell 4 for the DAC)

These macrocells can be used separately or together (see also paragraphs 1-3)

Figure 3 below gives the architecture of a stereo ADC and a stereo DAC built with the four cells.

The following paragraphs give some elements about the function of each macrocell:

Cell 1: the stereo delta-sigma modulators are second order modulators, Implemented with switched-capacitor integrators. The amplifiers have full differential structures. They are sampled at 128 x Fs. Analog inputs are differential. This cell contains its own voltage and current references. A stand-by mode is available.

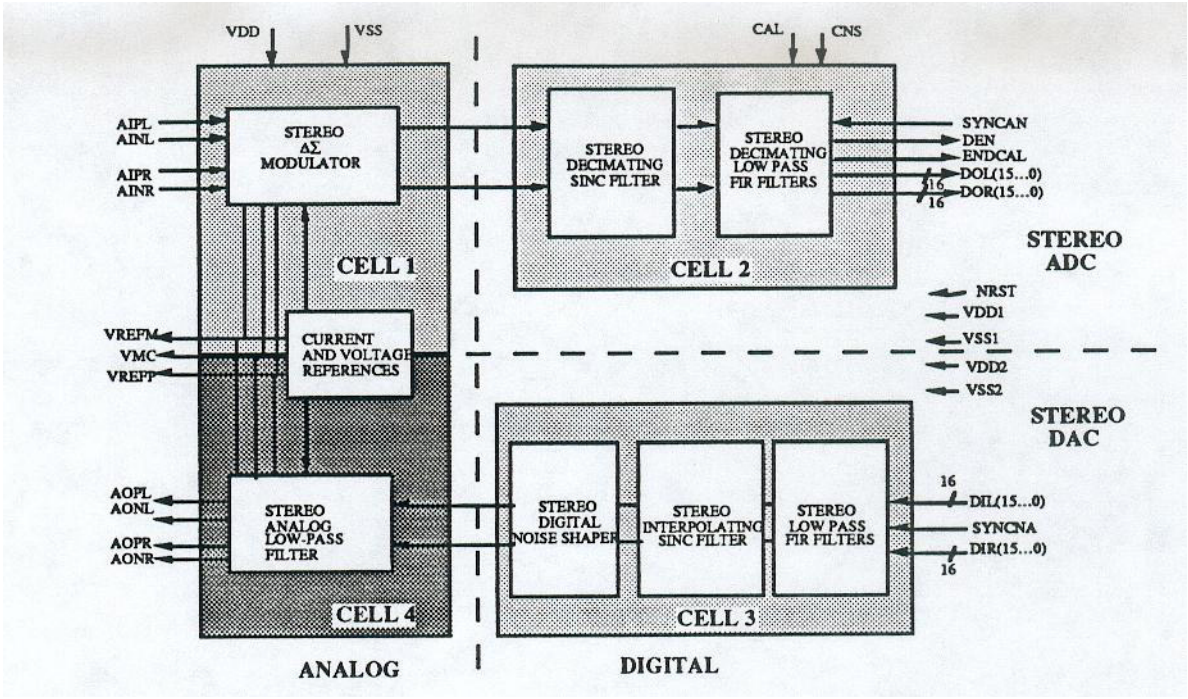

Figure 3 - Building a stereo DAC and a stereo ADC with the library macrocells

Cell 2: This macroceil contains two digital decimating filters per channel. The first stage is a sinc3 filter, with an oversampling ratio of 64. The second stage is a half-band FIR filter. The overall oversampling ratio is 128. The digital output sampling frequency is Fs; for example Fs = 44.1 kHz.

A stand-by mode is available.

Calibration

By using cell 1 and cell 2 together, two types of calibration, a "chip" calibration and a "system" calibration can be exercized through two appropriate inputs.

* In "chip" calibration:

The differential inputs of one channel are "short-circuited" internally to the internal reference voltage. The offset of the analog modulator only (cell 1) is measured.

* In "system" calibration:

The offset of cell 1 plus the offset of part of the analog conditioning is measured. This part is specified by the designer of the ASIC and can include either internal or internal and external analog conditioning.

In both cases, in calibration mode, a measure of converter offset is performed for each channel; the result is stored in an internal offset register for each channel. In the sequel, this stored values shall be subtracted from all samples computed by the second decimating filter before their output on DOR(15... 0) and DOL (15... 0) pins. The macroceil automatically returns to normal mode after some Fs clock periods.

Synchronization

The internal sequencers are synchronized with the signal SYNCAN. The only constraint SYNCAN has to respect is ensuring a frequency equal to Fs.

Cell 3: This macrocell contains all the necessary digital functions for a delta-sigma DAC, i.e. interpolating filters and a noise shaper which delivers to an analog low-pass filter a one-bit stream per channel. The interpolating filters have been implemented by cascading two half-band FIR filters and one sinc filter. The noise shaper is a second order modulator.

The internal sequencers are synchronized with the signal SYNCNA. The only constraint SYNCNA has to respect is ensuring a frequency equal to Fs.

Cell 4: This macroceil is an analog second-order low-pass filter implemented with a switched-capacitor structure. The outputs are differential. This cell contains its own voltage and current references. A stand-by mode is available.

All logic functions are implemented with static circuitry. Clocks can be stopped without any risk.

The four macrocells use CMOS transistors only, except for the reference voltage block which uses a bandgap with bipolar transistors.

This means that the macrocells can be easily ported to other CMOS or BICMOS technological processes, e.g. 0.7 gm (see paragraph 4).

1-2 ELECTRICAL CHARACTERISTICS

The technological process used is a BICMOS 1.2 gm with a single power supply of 5 V ±5 %, two polysilicon layers and two metal layers.

The main characteristics are given hereafter. These characteristics are obtained by using cell 1 with cell 2, and cell 3 with cell 4.

Typical analog characteristics

T = 25°C, VDD = 5 V, input sine wave of 1 kHz frequency, Fmclk = 11.289 MHz, measurement bandwidth 10Hz - 20 kHz, A-weighting filters.

Dynamic range:	80	dB
Signal to Peak Distortion	77	dB
Max gain mismatch between two channels	±0,25	dB
Gain @ 1 kHz	0±0,5	DB
Max offset error after calibration	100	LSB
Offset variation (function of Fmclk)	20	LSB
Maximum possible offset correction	± 80	mY

Filter characteristics

Frequency values are given for Fs = 44.1 kHz. If Fs is multiplied by a factor k, all frequency values are multiplied by k; the range for Fs is from 4 kHz to 48 kHz.

Parameter	Condition	Min	Typ	Max	Unit
Passband	± 0.25 dB	0		16.6	kHz
	-3 dB	20			kHz
Passband ripple	0-16.6 kHz	-0.25		0.25	DB
Stopband	-60 dB			26.5	KHz
Stopband attenuation				-60	dB

These specifications cover digital and analog filters.

1-3 "KIT-PART" CIRCUIT

A circuit, named ADDAC, has been designed to include the four macrocells described above. Together with these four macrocells, the circuit also includes:

- a serial interface to accees the 16 bit data (from the ADC or to the DAC)
- analog single-ended inputs or outputs
- analog differential inputs or outputs
- different programing modes allowing analog and digital loops, calibration modes and a stand-by mode. Some of these modes are designed for industrial testing of the macrocells.
- different power supply lines to characterize separately each function.

The block diagram of ADDAC is given in figure 4 below;

This "kit part" circuit is made available to users for a variety of purposes:

- characterization of the macrocells in different configurations and modes
- breadboarding of an application
- …

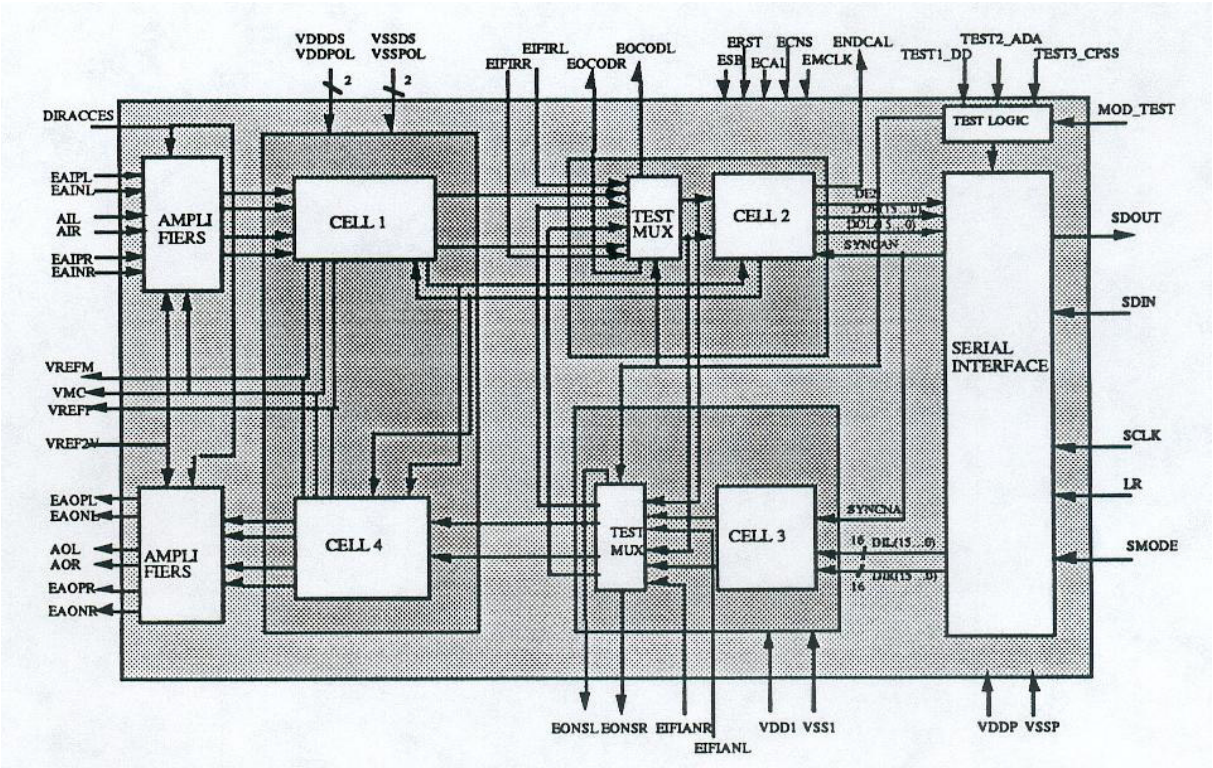

Figure 4 - ADDAC block diagram

2- METHODOLOGY FOR SPECIFYING SOME CHARACTERISTICS OF DELTA-SIGMA CONVERTERS.

Though they have become common for several years, delta-sigma converter characteristics and subtleties are not always obvious or easy to explain to unexperienced potential users. You will often encounter people who will state: "with this converter, my system works" or "with that one, it does not", but you will rarely encounter people who will state: "with such a specification my system will work" or "without such a specification, it will not work".

It is still quite useful to have the most accurate idea of what must be the right specification for a given application, because too severe a specification can lead to a low fabrication yield or to a high die cost while too relaxed a specification can lead to some misfunctioning under some conditions.

That is the reason why it is important to offer not only well characterized macrocells, like those described above, but also to offer the capability for designing different cells for specific applications and requirements. This is made possible and has been successfully experienced thanks to a programable delta-sigma ADC circuit, named OPALE.

This circuit had been designed by DOLPHIN INTEGRATION, a development center located near SGS-THOMSON in Grenoble, France. The OPALE circuit had been initially designed for military applications thanks to funding from the French Ministry of Defense (DGA/STEI).
Its block diagram is the following (Figure 5):

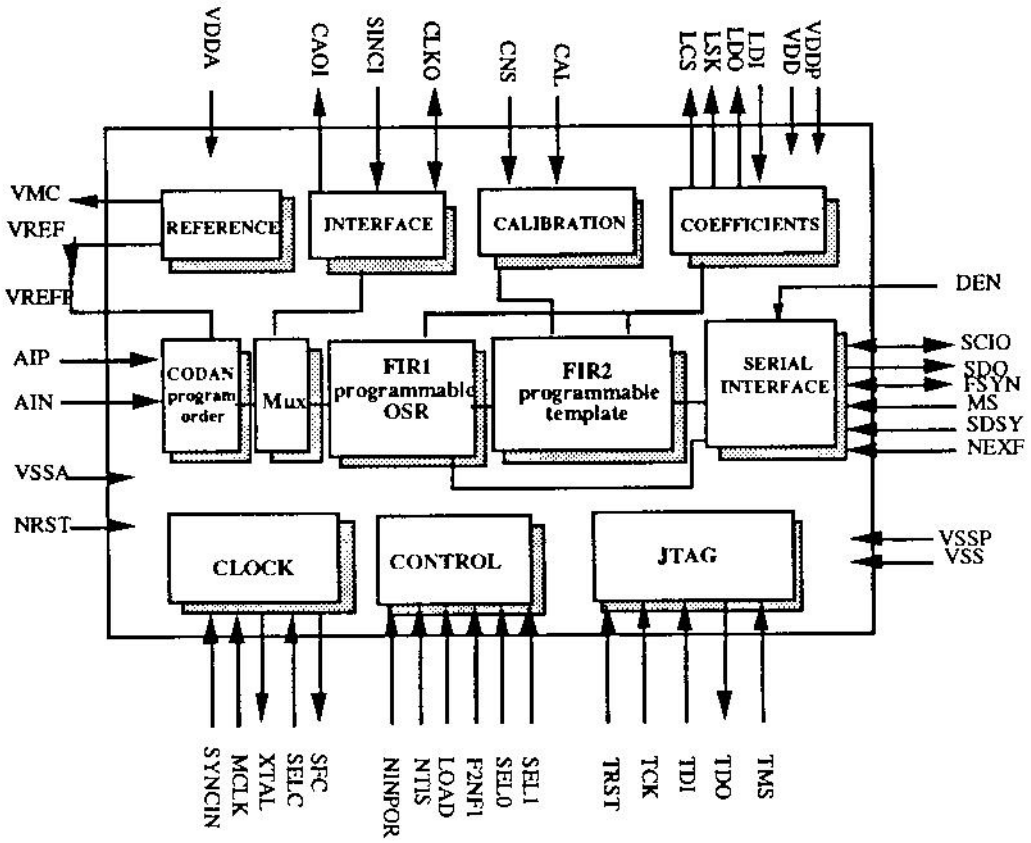

Figure 5 - OPALE block diagram

This monochip uses a CMOS 1.2 gin, 5 V technological process with one polysilicon layer and two metal layers.

The main relevant features here are the capabilities for programing:

- the order of the analog modulator is user-programable from 1 to 4,
- the oversamplig ratio of the first FIR filter (comb filter) is user-programable from 16 to 128,
- the template of the second FIR filter is user-programable by means of 256 coefficients of 20 bits.

All programing capabilities are available through a serial interface and the circuit can be programed just like a XILINX FPGA with an EEPROM connected to a microwire serial interface. Upon request, the EEPROM contents are loaded into OPALE which so becomes a user-specific programed circuit

With such a programable circuit, customers have the possibility to modify the characteristics of the ADC (SINAD, bandwidth, filters characteristics) and to measure the effects for their application. SINAD up to 90 dB have been obtained with OPALE in the audio bandwidth, and up to 98 dB is a lower bandwidth by using the modulator output only. Due to its high level of programability, the silicon area of such a circuit does not allow using it efficiently in high volume applications and specific macrocells have to be derived.

With such a methodology, required specifications can be quickly defined and checked for a given application.

We have applied it for designing the macrocells described above. The compatibility between the CMOS used in OPALE and the CMOS part of the BICMOS technology of SGS-THOMSON allowed reusing the basic cells without modification. Starting from the availability of specifications a delay of 4 months was sufficient to design the four macrocells (up to GDS2 tape and test vectors).

Such a methodology can be applied for every potential application.

3- CELLS LIBRARY FOR ANALOG CONDITIONING AND DIGITAL PROCESSING

The four macrocells described above have been included in a set of analog cells dedicated to multimedia applications. This set installed in the STKM3000 design kit includes several functions such as:

- Volume control attenuators
- Treble/bass correctors
- Automatic gain control
- Mixers
- Single ended to differential convertors
- Differential to single ended convertors

A schematic library of classical analog funtions such as amplifiers, comparatros, bandgap and power-on reset reduce the front-end development time.

For other analog functions not yet available, a library of devices included in the STKM3000 design kit running on the ADS environment (Analog Design System) make the design of personal functions easy. The possibility to extract an existing

schematic from the schematic library and the customization of it increase the flexibility with ADS.

A digital library of standard cells is used to design all the digital control functions.

4- FURTHER LIBRARY ENHANCEMENT

The STKM4000 series is the new library for mixed signal applications developped in the ANACA department of SGS-THOMSON Microelectronics. This standard cells library is designed in 0.7 gm BICMOS process. It will include for standard applications:

- A set of devices
- Up to 30 analog standard cells such as op amp, comparators, voltage reference, oscillators...
- A digital standard cells library (90 internal cells and 80 peripheral cells)

To expand the application field toward multimedia and telecommunication, the DELTA-SIGMA macrocells will be redesigned in 0.7 gm process.

A complement of macrocells will expand the function set:

- Core of microprocessor
- SPRAM, DPRAM and ROM generators
- UART and timers
- 12 bits A/D successive approximation converter
- 10 bits AID and 9 bits D/A video converters

This new library will be implemented into a new Analog Design System (ADSO5) running on ARTIST environment from CADENCE.

5- CONCLUSION

A set of techniques, cells and circuits for the specification and design of multimedia ASICs including delta-sigma audio converters has been presented. It includes:

- Delta-sigma DAC and ADC macrocells
- A stereo delta-sigma DAC and ADC kit part circuit
- A programable delta-sigma ADC circuit
- A set of analog and digital cells for various functions

With such tools, ASIC designers and users can have a quick development time, a high security in the good working of new complex designs and the best performances for the right price.