Performance of high resolution analog functions embedded into a SoC guaranteed by the Three-Noise-Path method

Introduction

System-on-Chip (SoC) integrators have to put in place appropriate verifications in order to guarantee performance of analog Virtual Components (ViCs), also called IP blocks, once integrated into the SoC.

Such performances may be affected by various kinds of noise and the most critical issue in integrating analog functions is then to assess potential noise sources, to control noise propagation channels through the SoC and to evaluate noise impact at the interface between the ViC and the rest of the SoC.

Due to exponential increase of SoC complexity, flat simulation at top level is not achievable with the appropriate level of accuracy. And the question becomes how to ensure high performances for analog functions taking into account their environment within the SoC?

Thus innovative simulation methods and models have been developed and qualified on silicon to allow SoC Integrators performing noise simulation of their SoC and then assessing the real performance of embedded analog ViCs at SoC level.

1. A new SoC modeling through the Three-Noise-Path method

The main challenge in verification for a SoC integrator is to take into account all the noise effects in simulation within reasonable time and resources. To handle this problem, the purpose is to focus on noise impact and to build a noise model for the SoC.

The first step is to partition the SoC in order to identify the potential noise sensitive ViCs, the “victims”, the potential noise sources, the “aggressors” and the propagation channels between such aggressors and the victims.

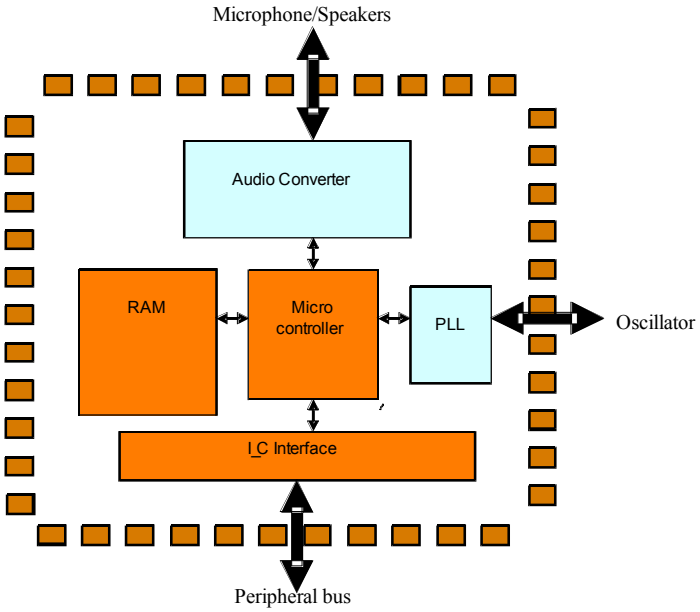

Figure 1. Example of mixed signal SoC

Figure 1 shows a simplified example of a mixed-signal circuit. In this example, the microcontroller accesses to RAM, as well as I²C interface can be considered as potential aggressors (orange blocks). Indeed, sensitive analog blocks (in blue) such as the PLL or the audio converter may be impacted by the switching activities on I²C bus or RAM data bus.

To help SoC Integrators, three noise paths have been identified:

- the VDD/VSS noise path, composed of:

  an emitter, which can be current peaks from digital block switching,

  propagated through the parasitics impedances of power and ground nets

  till analog devices power supply

- the VSS-substrate noise path:

  an emitter, which can be current peaks from digital block switching,

  injected on substrate impedances through substrate taps

  till analog devices substrate taps

- the IO-Ring noise path:

  an emitter, which can be current peaks from digital IO switching,

  propagated through IO-Ring impedances

  till analog signals inputs

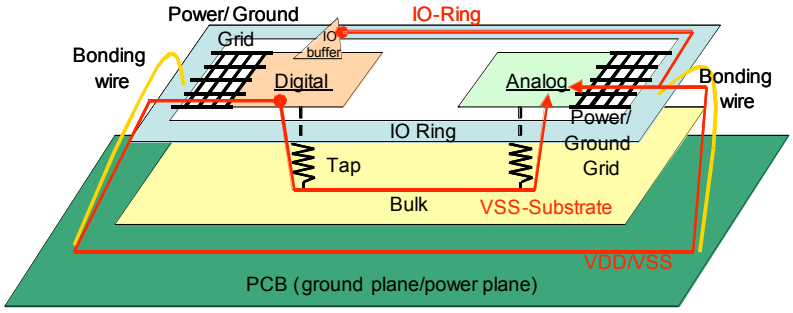

Figure 2. Three-noise-path schematic

These three noise paths are valid whatever the mixed-signal circuit and whatever its application.

2. A new simulation approach

The second step is to define the set of simulations to be run: choice of the appropriate simulation model of the ViCs with the relevant simulation level.

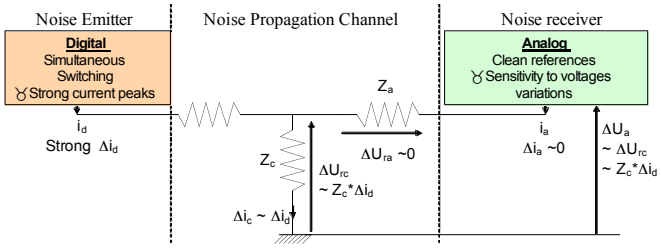

Figure 3. Simplified small-signal schematic of a noise path

Figure 3 shows how a noise path can be split: each noise path is composed of an emitter, a propagation channel and a receiver.

In the sequel, details of the method will be described for the VDD/VSS noise path; it is characterized by:

- Noise emission: current peaks from digital blocks switching. In digital blocks, clock edges are propagated to a large amount of synchronous gates. This cumulated number of commutations can generate high current peaks between power and ground connections

- Propagation channel: parasitics impedances of power and ground nets (such as routing impedances, bonding wires and power decoupling). These nets, by conducting digital high current peaks from digital part, are producing voltage variations on common nodes.
- Noise receiver : high performance analog are usually sensitive to reference and power local variations

As simulation of the full noise path could still be heavy, simulation can be divided in three parts:

- Part 1 - Generation of Emitter noise profile:

  For a VDD/VSS noise emission, a simple power simulation with an EDA solution like SCROOGE easily provides current peaks of noise emitter from:

  A Post-layout Netlist and Standard Delay File

  A Testbench reflecting "noisy" configuration of the emitter

  The Liberty file of Standard cell library

  The noise profile, represented by the $I_{total}=f(t)$ wave resulting from this simulation has then to be transformed in the frequency domain (by a Fast Fourier Transform, for practical purposes)

- Part 2 - Simulation of channel filter with noise profile as input (the result of this simulation will be seen as inputs by the receiver):

  Current peaks with propagation channel main impedances are simulated in small signal.

  For a VDD/VSS noise channel, the main parasitics components encompass the capacitance of internal decoupling, the resistance of power and ground routing paths, the inductance of bonding wires on power and ground, the capacitance of external decoupling, the output Capacitance of Power Supply (Frequency compensation of external regulator, for instance)

  Note that the noise receiver will not see high frequencies as VDD/VSS noise channel is a low pass filter. As a consequence, the simulation for establishing the noise profile (part 1) does not need necessarily to be instant-current accurate but charge accurate ($q(t)=\int i(t).dt$).

- Part 3 - Comparison of Filtered noise profile Versus Receiver Tolerance template from IP provider

  In the case of the VDD/VSS noise path, the receiver sensitivity, depending on frequency of the Power Supply noise is given by *Power Supply Noise Tolerance Template*. This template is in fact an extension to other frequencies of the *Power Supply Rejection Ratio (PSSR),* traditionally used in industry.

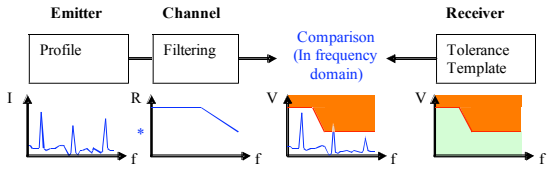

Figure 4. Profile Versus Tolerance template comparison

Then a complex time and resource consuming simulation has been reduced to a couple of simple simulation per noise propagation channel plus a comparison between a profile and a template in frequency domain.

3. A silicon qualified method

In order to assess the equivalence between these simulations and silicon results, a silicon qualifier named CORSAIR has been launched. Several devices have been implemented on this silicon to allow noise emission and reception through the three channels described in this article:

- As noise receivers:
  - A low power 95-dB audio Digital Analog Converter (DAC) - product named Helium - to validate its performance and its resilience to VDD/VSS and to IO-Ring noises (Helium is supposed to be totally resilient to VSS-Substrate-noise)

- A high gain large-band analog amplifier designed as a VSS-substrate noise sensor to validate our VSS-substrate noise propagation models using several layout configurations: with and without guard ring, with and without transistor matching…

- As noise emitter, a patented specific block, named STRIDE, has been designed. STRIDE is a digital noise emulator, divided in three specific parts, one per noise channel. Each part is able to emit a programmable noise then allowing to isolate noise propagation on the selected channel:
  - STRIDE-CORE-VDD/VSS is a set of short-cut switches that can be enabled or disabled individually depending on the VDD/VSS noise profile to emulate
  - STRIDE-CORE-VSS-Substrate with the same kind of switches used in STRIDE-CORE-VDD/VSS, plugged to the substrate with substrate taps allowing the injection of a VSS-Substrate noise profile
  - STRIDE-IO is a set of high drive digital IOs with programmable inputs

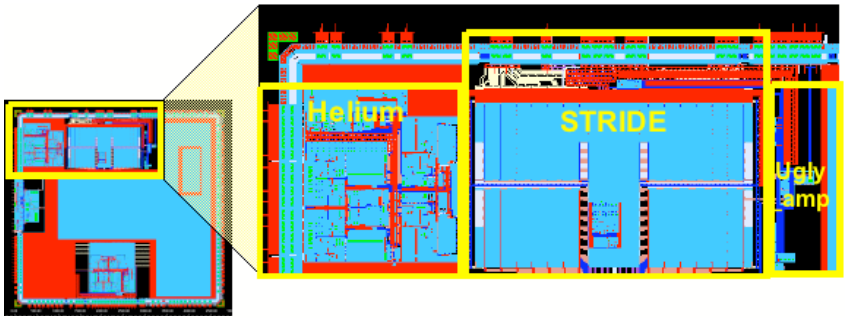

Figure 5. CORSAIR layout

Conclusion

This paper has proposed a simple but efficient noise modeling of a mixed-signal SoC through three noise propagation paths: VDD/VSS, VSS-Substrate and IO-Ring. This allows the simulation of high performances analog functions by taking into account potential disturbances of the rest of the SoC.

Each simulation of a noise can also be simplified by comparison between propagation channel filtering of noise emission profile and noise receiver tolerance template.

A silicon qualifier containing three different noise emitters has been manufactured to permit correlation of simulation results with Silicon measurements.

Then, performance loss for sensitive devices in a noisy environment is now simulable by designers at SoC level, thanks to its noise model built as an assembly of noise emitter/channel paths. This allows prediction of a component performance once integrated in a SoC.

More information available on demand:

- on Dolphin website: http://www.dolphin.fr/emp_services/socintegration/soc_integration.php
- by e-mail: logic@dolphin.fr, soc.commercial@dolphin.fr

About the Author

Florian Espalieu received a master's degree in electrical engineering from Phelma (ex-ENSERG), Polytechnic National Institute of Grenoble, France, in 2003. He joined Dolphin Integration the same year. After three years spent on the development of SATA high speed data links, he is now in charge of noise simulation in mixed signal SoC. He is holder of a patent on analog test device.