

Calibration in a MEMS based measurement system or how to make a sensor-ASIC loop of high resolution work

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Micro-Electro-Mechanical Systems (MEMS) as inertial sensors, like accelerometers and gyroscopes, are finally becoming attractive for many industrial applications, and their potential range of use is about to explode in the coming years. The application trend towards high resolution, reliability, and miniaturization, pushes system integrators to combine both the inertial sensor and its application-specific integrated circuit (ASIC) in a force-balanced feedback arrangement, implemented as a single System-in-Package (SiP). The real challenge then consists in guaranteeing both performance and yield for the overall SiP. The system integrator must acknowledge that design flow and fabrication techniques are different for the mechanics and the electronics: MEMS sensor design relies on finite-element simulation to model electrostatic effects, whereas electronics must take into account worst-case corners of process steps and of operating conditions, voltage and temperature, with SPICE-like simulations. Managing the design of mixed electronic-mechanical systems thus requires a common simulation environment, with specific models the fidelity of which to sub part of specifications must be assessed.

1 Coupling mechanics and electronics

Successfully designing such a high performance system is not only a matter of getting the best performance from each individual part, but also a matter of understanding the interactions between mechanics and electronics. Figure 1-1 illustrates a simplified diagram of a sigma-delta force-balanced feedback loop for a MEMS accelerometer. The sensor is made of a mobile mass which moves along the sensing axis in response to an external acceleration, and two fixed electrodes for electrostatic feedback actuation. A first electronic stage converts the sense capacitance variations into an electrical signal, while a second stage provides gain to improve noise shaping. A single-bit quantizer converts the analog signal into an over-sampled one-bit sequence.

The feedback path consists in a one-bit DAC which applies a differential image of the output bit-stream onto the sensor feedback electrodes, such as to create a force that opposes the initial acceleration.

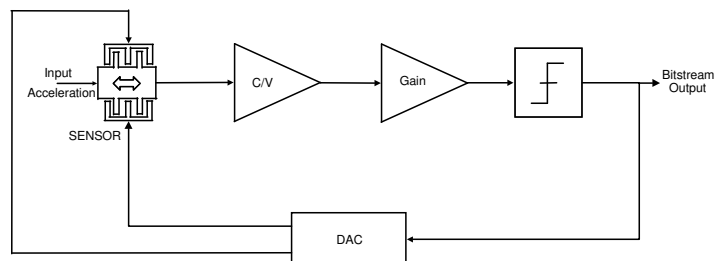


Figure 1-1: sigma-delta feedback Loop

1.1 Accelerometer impact on stability

The sensor characteristics strongly affect the system feasibility, performance and implementation. For an accelerometer inserted in a force-balanced feedback loop, the architect has to consider sensor parameters like mass, stiffness constants, noise floor, and dc gain, in both open loop and closed loop to ensure the system reliability.

As shown in Figure 1-2, high quality-factor sensors present secondary resonance frequencies caused by the movement of mobile and fixed fingers, which can jeopardize stability. The loop instability which they may cause is explained by the 180° phase change around the secondary resonance frequency.

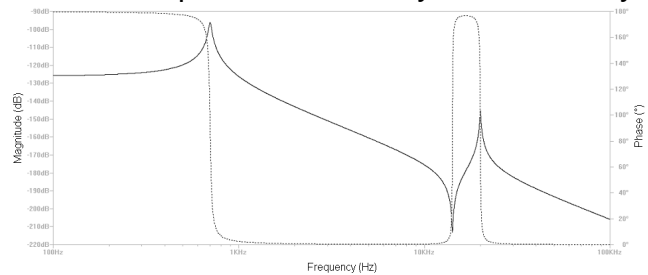


Figure 1-2: Frequency response of the mass displacement to the feedback force

To alleviate the risk associated with secondary resonances, the approach consists in investigating their impact by measuring, via simulation, the closed-loop SQNR for different frequencies and Q factor. The purpose of this analysis is to provide the MEMS manufacturer with template boundaries of secondary resonance frequencies and Q factor to guarantee SNR and stability. Seeger [1], has shown that in the case of collocated sensors (the same fingers are used to sense acceleration and apply the electrostatic feedback force), the secondary resonance frequencies should be below $F_s/6$, F_s representing the sampling frequency.

1.2 Budget distribution from noise sources

The sensor main resonance frequency and DC gain vary with the magnitude of the force feedback voltage due to electrostatic spring effects [2], which may over-constrain the electronics connected to the sensor output.

The identified noise contributors in force-balanced accelerometers are mechanical Brownian, front-end amplifier, kT/C , reference voltage, and quantization noise [3]. When targeting high resolution systems, another noise source that should be taken into account is the clock jitter. Many components in the loop, such as feedback DAC, demodulators, integrators and differentiators, are sensitive to clock jitter, which introduces noise in the loop and reduces the dynamic range. The proposed approach allows specifying a "jitter tolerance template" to fix the acceptable level of jitter which guarantees the dynamic range specification from simulation results.

2 A Multi level virtual verification chain to guarantee the performances of the overall system on silicon

The key solution resides in the simulation environment: it is mandatory to represent all mechanical and electrical coupling domains to get a homogeneous overall behavioral model. It implies the assessment of the tolerance margin of each domain, to the acceptable fabrication variations of the other. Each domain is used to its specific language, simulation and measurement methods. The multi-level simulator SMASH™ [4] can simultaneously handle both analog/mixed-signal structural models and high level languages such as VHDL-AMS, so that mechanical and electronic

behavior can be modeled in a coherent framework, using physically meaningful parameters.

2.1 Modeling a sensor

In contrast to classical object-oriented electromechanical modeling, i.e. describing plates, suspensions, drives, etc., models of basic physical effects have been combined with object models which in turn can be used for system modeling. This allows to freely choose which effects are to be considered for each type of simulation. Moreover, the development of new object models is simplified, as in [5]. The VHDL-AMS implementations of these effects were taken from the library EMBLEM-Mecha of Dolphin Integration.

With such modeling, sensitivity analysis, optimizations and robustness analysis of the sensor are readily made available.

2.2 A multi level verification with Equivalence Checking

With multi-domain systems, simulation complexity may increase considerably, leading to unpractical simulation times at SPICE level and potentially false results.

The hierarchically structured approach consists in a multi-level verification chain using different levels of modeling: for instance, using a high-level modeling language such as VHDL-AMS to verify the loop stability, to perform jitter simulation of the loop, and to provide the acceptable level of jitter that guarantees the dynamic range specification for a given architecture; while only using SPICE simulations for sub elements of the architecture in order to guarantee by design the overall performance. Indeed, two approaches are confronting, bottom-up for analog design and top-down with behavioral libraries for the system integration: then, it is essential that modeling at both levels be consistent. In order to ascertain such consistency, point-wise equivalence classes must be specified and "Equivalence Checks" must be applied. Typically a PLL is characterized by its locking time which serves as Equivalence Check between the electrical and functional levels of modeling; similarly distortion of a DAC output stage in db serves as Equivalence Check for its harmonic amplitude.

2.3 Virtual testing to determine the method of the industrial testing

The tester configuration involves a basic choice where cost trade-offs are involved between investment expense and test duration: as a matter of fact Testability analysis merely is about the practicality of the tester configuration; it is mandatory to ask the question whether any performance can be measured.

It is recommendable that the system integrator chooses an equipment configuration at an early stage to be in position to perform virtual test prior to fabrication.

3 Towards an industrial goal with a calibration platform

The Characterization, distinct stage from Testing, confirms whether the system is ready for mass production with an acceptable yield to meet commercial aspects as well as the requirements for reliability and performance over the product life.

MAPLE is a hardware programmable station with a silicon ASIC and sensor electrical emulator, containing a set of tools and solutions for calibration. This is a mean to predict the performance of the complete system, considering the calibration process

as part of the design. The required performance then dictates the acceptable range of parameter spread, thus leading to an acceptance test for the fabricated MEMS. This calibration platform enables to assess the sensitivity of each circuit to the system environment. It allows programming dynamically the architecture elements to achieve stability and best noise-shaping. By emulating the sensor and electronics corners, it is possible to find out the acceptable variation range in which the system is in conformity with the specifications. The prototype acceptance is then more thorough and faster.

4 Summary

The best way to verify system of high-resolution ($\mu\text{m}/\text{G}$) with sigma-delta micro-accelerometer architecture has been presented. Our approach permits to define required simulation models and simulate all MEMS and electronics coupling fields to guaranty the robustness of the complete system.

5 References

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