A current mirror model in Verilog-AMS

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Abstract

This work presents a model of a simple current mirror implemented in Verilog-AMS language using the circuit simulator Smash. The model is validated through comparisons with simulations made with the ACM model implemented in Smash. Simulations with the current mirror used to bias a Differential CMOS Amplifier is shown in order to illustrate the model's functionality.

1. Introduction

Verilog-AMS is an extension of IEEE 1364 Verilog Hardware Description Language (HDL) specification. It has made Analog and digital circuits much easier to design and simulate, because the simulations are quicker and the language itself is richer than Spice [CHE 03]. For these reasons, we intend to write analog circuit models in Verilog- AMS HDL, as it has been done to digital circuits. This work shows an example of a model for the current mirror shown in fig.1.

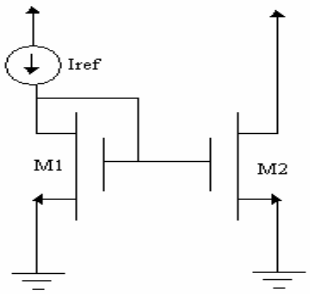

Fig. 1 – Current Mirror

2. The Current Mirror Model

To model the simple current mirror, a model of MOS transistor valid for strong inversion was used [ENZ 95]. In the linear region the drain current of the MOSFET is given by:

$$I_d = \frac{1}{2}\mu C'_{ox} n \frac{W}{L}\left[(V_p - V_{sb})^2 - (V_p - V_{db})^2\right] \quad (1)$$

Where V_p is the pinch-off voltage, V_{sb} is the source-to-bulk voltage, V_{db} is the drain-to-bulk voltage. μ, n, C'_{ox} and W/L are the mobility, slope factor, gate oxide capacitance by area and the transistor aspect ratio respectively. In the saturation region, the drain current is:

$$I_d = \frac{1}{2}\mu n C'_{ox} \frac{W}{L}(V_p - V_{sb})^2 \quad (2)$$

To make the model become continuous with a smooth transition between the triode and saturation regions an interpolation function (equation 3) was used in the MOS model [JOA 98].

$$V_{db} = \frac{V_{ds}}{\left[1 + \left(\frac{V_{ds}}{V_p}\right)^{2k}\right]^{\frac{1}{2k}}} + V_{sb} \quad (3)$$

In (3) V_{ds} is the drain-to-source voltage and k is a parameter that can be adjusted, in this case it was adjusted to unity. The early effect was modeled linearly, multiplying equations (1) and (2) by the factor $1 + \frac{V_{ds}}{V_A}$, where V_A is the Early Voltage.

The input parameters for the current mirror are the transistor width and length, and the technological parameters of the process. The variables are the reference current, at the input, and at the output, the output current and resistance. The VERILOG-AMS code is shown in the appendix.

3. Results

To check the validity of the model it was compared with simulations done using the ACM model, implemented in SMASH, for several values of the reference current. The results are shown in figures 2 to 4.

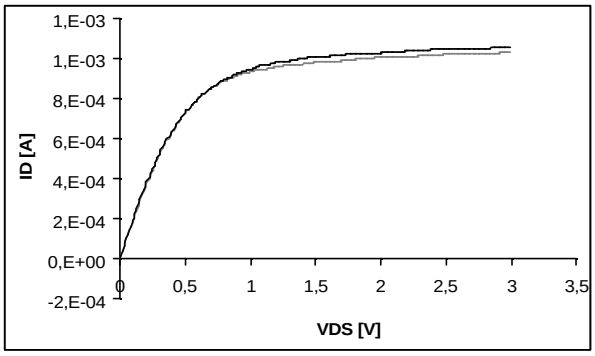

Fig. 2 – The output current of the mirror for a reference current of 1mA. Model in VERILOG-AMS (black) and ACM model (gray).

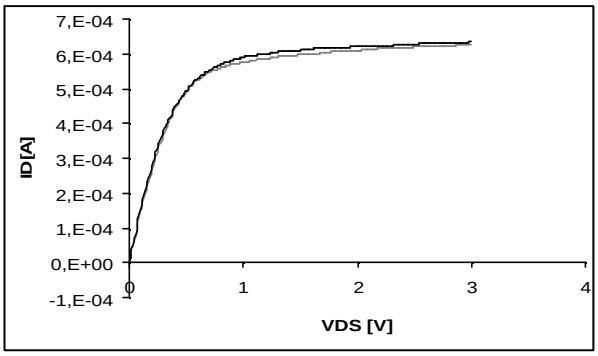

Fig. 3 – The output current of the mirror for a reference current of 600uA. Model in VERILOG-AMS (black) and ACM model (gray).

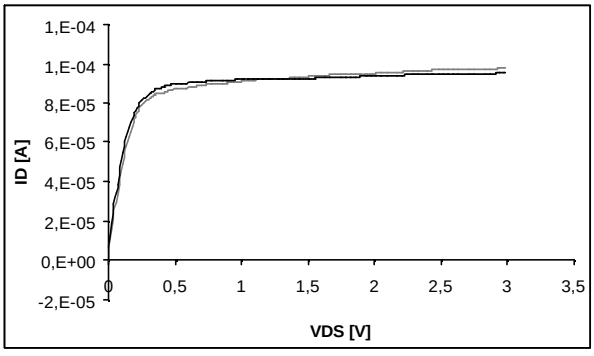

Fig. 4 – The output current of the mirror for a reference current of 90uA. Model in VERILOG-AMS (black) and ACM model (gray).

In order to illustrate the usefulness of the model in the simulation of more complex circuits, it was used as the bias circuit of a differential amplifier as shown in figure 5.

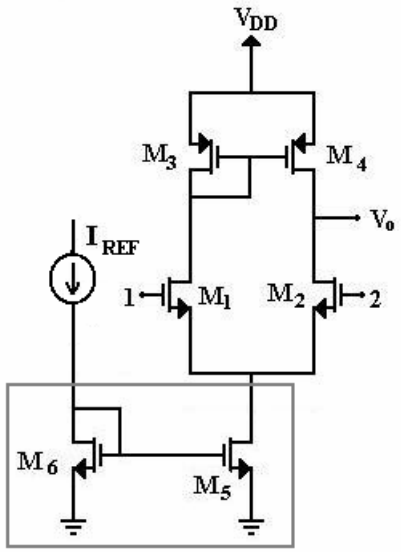

Fig. 5 – CMOS differential amplifier biased by a current mirror

Figure 6 shows the comparison of the transfer characteristics of the differential CMOS amplifier using the VERILOG model for the current mirror with the same amplifier simulated with all the transistors modeled by the ACM model.

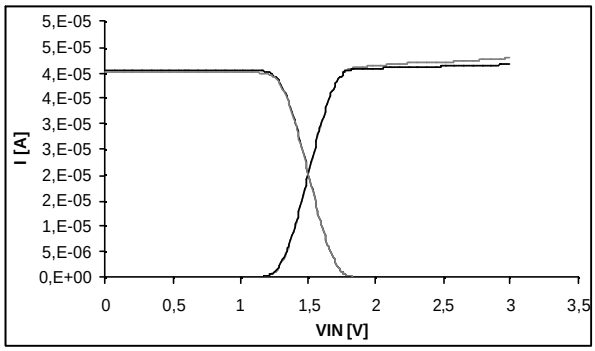

Fig. 6 – The differential CMOS amplifier transfer characteristics, with a bias current of 40uA, using VERILOG model for the current mirror (gray) and with all the transistors simulated with the ACM model.

4. Conclusion

In this work, the simple current mirror presented in fig. 1 was modeled using Verilog-AMS HDL. Simulations using this model agreed well with those using a more complex model for the transistors. It is also an example of how simple and useful is to write analog building blocks with an analog HDL.

Acknowledgments: The authors would like to thank Dolphin Integration, especially Gilles Depeyrot for licensing SMASH Simulator.

5. References

[ENZ 95] Enz C. C., Krummenacher F., and Vittoz E. A., **An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications**, Analog Integrated Circuits and Signal Processing Journal, vol. 8, pp. 83-114, July 1995.

[JOA 98] Joardar, K., Gullapalli, K. K., McAndrew, C. C., Burnham, M. E., and Wild, A. **An Improved MOSFET MODEL for Circuit Simulation**. IEEE Transactions on Electron Devices, vol. 45, nº 1, pp. 134 –148, January 1998.

[CHE 03] Cheng, K., and JOU, K. F. **2.4GHz CMOS VCO Design with VERILOG-AMS.** ICM 2003, pp. 98 -101, December 2003.

Appendix

This appendix shows the current mirror model implemented in Verilog-AMS language using the circuit simulator SMASH.

```
>>> VERILOG
`include "…/packages/disciplines.vams"
`include "…/packages/constants.vams"
`timescale 1s / 1fs
////////////// current mirror ////////////////
module mirror(t1,t2);
electrical t1, t2;
inout t1,t2;
parameter W=20u,L=1u,Vsb=0,Iref=1m;
real n,u,c,kn,Vp,VpVsb,den1,den2,Vdb,Va,Vto,x,k,p1,p2,Vg;

analog begin


 n=1.3;
 u=4.035e-2;
 c=4.48e-3;
 kn=0.5*n*u*c*(W/L);
 x=L/1u;
 Va=50/x;
 Vto=0.4655;
 k=1;
 p1=2*k;
 p2=1/p1;

 Vg=(sqrt(Iref/kn)+Vsb)*n+Vto;
 Vp=(Vg-Vto)/n;
 VpVsb=Vp-Vsb;
 den1=1+pow(V(t1,t2)/Vp,p1);
 den2=pow(den1,p2);
 Vdb=V(t1,t2)/den2+Vsb;

I(t1,t2) <+
kn*(pow(VpVsb,2)-pow(Vp-Vdb,2))*(1+V(t1,t2)/Va);

end

endmodule
```