DOLPHIN INTEGRATION

Effective Optimization of Power Management Architectures through Four standard "Interfaces for the Distribution of Power"

Abstract

In the promising market of the Internet of Things (IoT), System-on-Chips (SoCs) are facing exponential design complexity challenges and ultra lower power consumption requirements. The architectural definition, component selection and integration of power management play a major role in the quest of device minimization and battery lifetime maximization.

In order to reach the best Return on Investment (RoI) and Time-to-Market (TTM), Dolphin Integration launch the disruptive approach of a DELTA Reusable Power Kit Library (RPKL) for building power management architectures with reusable regulation components. The concept of Figure of Merit (FoM) is introduced for the RPKL approach to select the optimal power management solutions per application requirements with the best trade-off among diverse performance criteria, be it power consumption, silicon area or Bill-of-Material.

The standardization of four Interfaces for the Distribution of Power (IDP) is a sine qua non condition of the RPKL approach, as it leads to reusable regulators and allows a smooth combination with in-house or third party regulators. The selection of the four voltage levels and their range of accuracy is explained and the benefits are provided.

Finally, the seven rules of the DELTA standard are shared and, as long as any regulator is designed per these rules, it can partake in the optimal power management solutions with the best management of integration risks through EDA simulation and verification.

In the golden era of M2M (Machine to Machine) connected world, IoT (Internet of Things) is the new buzzword to designate all the ubiquitous "smart things" that can be interconnected to other things/devices/objects. Typical IoT applications can be smart wearables and smart home appliances.

Due to the increasing features and decreasing device size for smart portable devices, the System-on-Chips (SoCs) for IoT are facing exponential complexity with stringent power consumption (dynamic power and leakage) and low Bill-of-Material (BoM) requirements. Fabless companies for IoT applications are all trying to reduce the overall power consumption using different techniques such as Dynamic Voltage and Frequency Scaling (DVFS), multi-voltage power domain, state retention…

The critical and important approach to achieve ultra low power requirements is to thoroughly define the right architecture of SoC or subsystem with different voltage and power domains, together with the integration of the Power Management Network (PMNet) enabling low power design techniques and BoM reduction.

The PMNet is the network containing all the regulation components (regulators, passive filtering components, physical nets such as power grid and its parasitic elements) from the power source to each different load/block in the SoC or subsystem. The PMNet architecture is traditionally optimized bottom-up for each load in a SoC, partaking in a hardly reusable library. There can be as many PMNet as there are applications. Therefore, one of the main challenges for SoC integrators is to select the appropriate PMNet architecture per application requirements and to embed the right regulators.

This article suggests an innovative approach to build an optimal PMNet per application requirements, based on the definition of four standardized voltage levels (further defined as Interfaces for the Distribution of Power). Finally, it demonstrates the advantages of this approach from which regulator suppliers or designers, SoC integrators and system makers can benefit.

DELTA: the Disruptive approach of the Reusable Power Kit Library (RPKL)

Instead of using as many custom regulators as needed in a complex SoC design, which would lead to higher design or purchasing costs and longer Time-to-Market (TTM), the RPKL approach is recommended to SoC integrators in order to:

- Design or acquire a kit of reusable components for controlling the lead-time from LEF-freeze to Tape-out, hence reducing the TTM,
- Enable diverse optimizations (e.g. high efficiency, low noise, low BoM, low leakage…) with a reduced set of components for each criterion,
- Promote rules for standardizing PMNet integration so that the PMNet can be comprised of cooperating regulators from competitors and partners alike for seamless integration and assembly.

The concept of Figure of Merit (FoM) is also introduced by the RPKL approach to select the optimal PMNet per application requirements. With custom regulators, users tend to compare the performance of each different custom regulator and have no clue to compare the PMNet architecture solutions as a whole. On top of that,

applications often target a specific trade-off among different optimizations; let it be low power, low BoM or low noise. Thanks to a specific FoM, it is then possible to identify the best PMNet architecture among others for a given SoC or subsytem.

The Figure-of-Merit (FoM, the lower the better) is an arbitrary function assigning weights to various parameters in order to optimize a mix of performances. The SoC integrator then only needs to make a choice of performance trade-offs between area, BoM, leakage, dynamic consumption…

An example of PMNet benchmarking using a FoM will be shown later in this article.

The Need for a standardized Interface for the Distribution of Power (IDP)

In order to define reusable and flexible regulators, the use of several pre-defined and standardized Interfaces for the Distribution of Power (IDPs) is necessary. An IDP is an interface through which the power is distributed to diverse power islands or loads. A one-to-one connection simply is an Interface for the Attribution of Power (IAP).

Once the IDP is defined, it is then possible to divide the regulation constraints between upstream and downstream regulators. The IDP level is defined by limited voltage ranges and a maximum noise spectrum which can be tolerated on the IDP by the downstream regulators and its loads. As shown in Figure 1, upstream regulators are the ones directly connected to the power source (Li-ion battery or USB 5 V), so they need to have high-voltage protection, while the downstream ones are connected to the loads and shall be optimized for each load or power domain's requirements (e.g. low leakage, low noise for RF or analog block…). It also enables trade-offs between higher conversion efficiency, area, BoM and the need for noise immunity in SoCs embedding many power domains.

The definition of these IDPs is the sine qua non condition of the RPKL approach as it leads to reusable regulators and smooth combination of in-house or third party regulators.

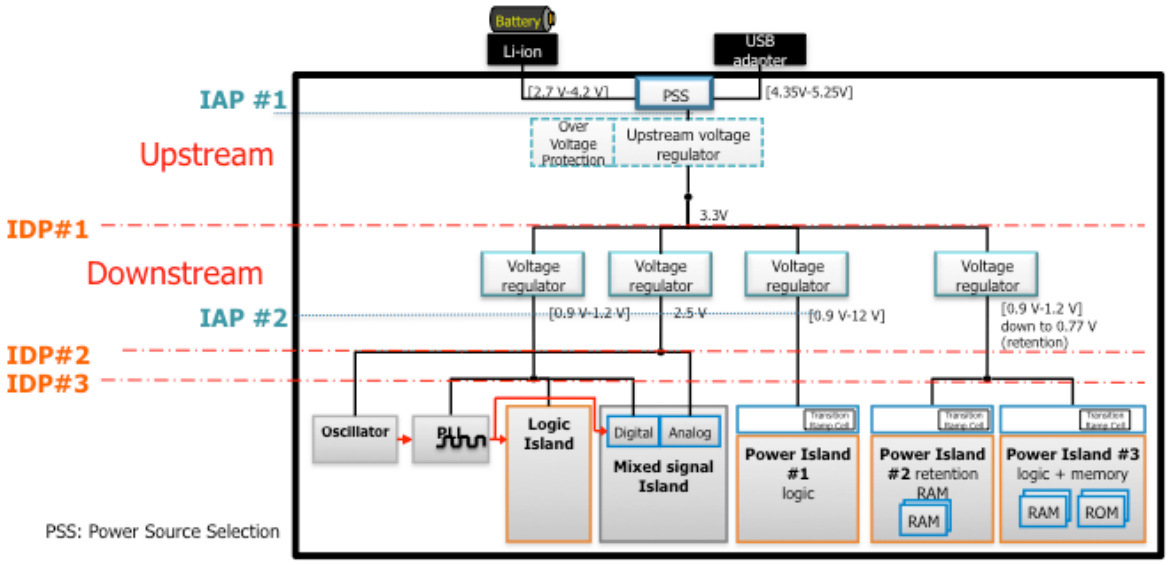

Figure 1: Separation of upstream and downstream regulators thanks to IDP

The "Fantastic Four" IDPs

After analyzing tens of block diagrams for diverse IoT applications - such as smart metering, smartcard, smartphone, smart glass, tablet, smartwatch -, from 180 nm to 28 nm, 4 different IDP voltages are the minimum necessary and sufficient number to build an RPKL.
As shown in Figure 2, from technology nodes 180 nm down to 40 nm, the selected voltages are 1.2, 1.8, 2.5 and 3.3 V. For 28 nm and 16 nm, there are still 4 IDPs but with different voltage levels. These IDPs thereby set the standard for regulator input and output voltages.

The reasons for selecting these 4 voltages are:

- Common voltages in systems, supply I/Os and peripherals for technology nodes across 180 nm, 90 nm, 65 nm, 40 nm and below,
- No IDP higher than 3.3 V (+/- 10%) down to 40 nm to avoid high voltage protection for downstream regulators in order to minimize silicon area,
- Overall optimization can be found with regulators based on these IDPs instead of customer regulators with different interconnection voltages,
- Adding one more IDP would not lead to better overall PMNet optimization but will for sure lead to the superfluous increase of regulator components within the RPKL.

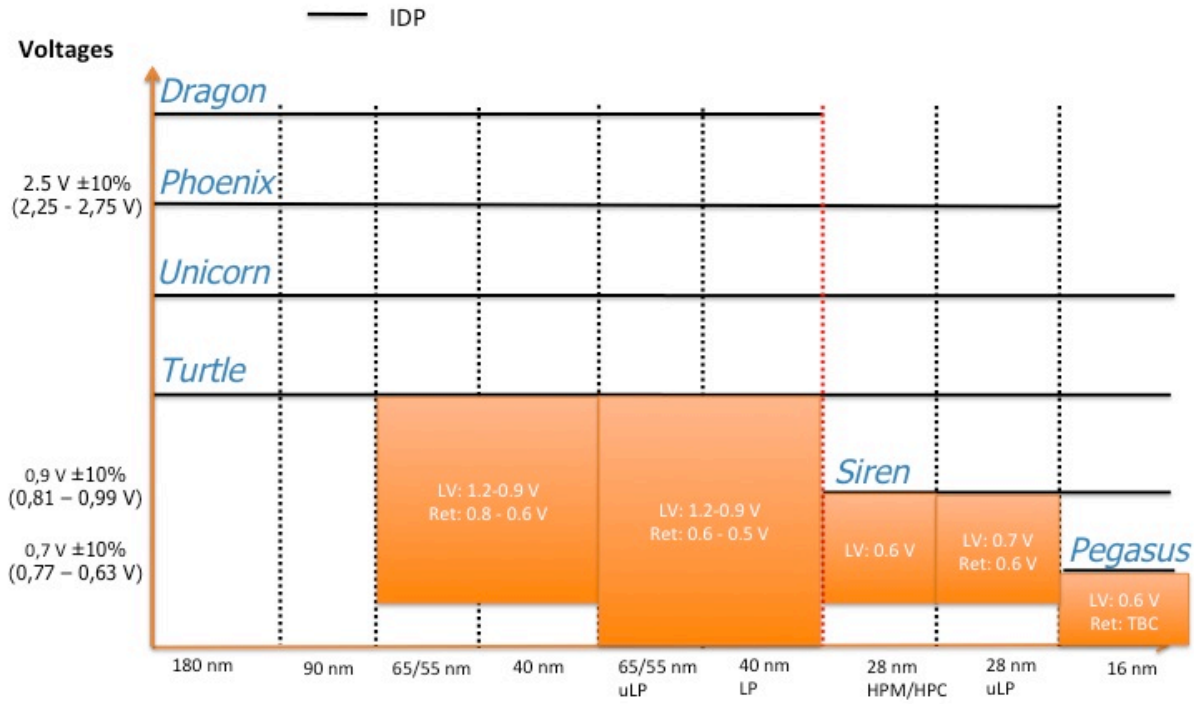

Figure 2: IDP voltage level per technology process

Overall SoC Optimization thanks to RPKL with standardized IDP

Let's take the example of a smartwatch application (with the simplified block diagram as shown in Figure 3) for illustrating the difference between RPKL (based on defined 4 IDPs) and custom regulators (as referred to CPKL – Custom Power Kit Library, using other voltage level – 1.4 V – for cascading regulators).

We assume that this SoC is in stand-by mode (Always-on block active only) during 99 % of lifetime operation. As we want to minimize the average power consumption and silicon area, we can use a simplified FoM, which is the average power consumption multiplied by the silicon area of the embedded regulators (FoM = mWh * mm^2). The power efficiency of the switching regulators (SR) is assumed to be 80 % in both cases.

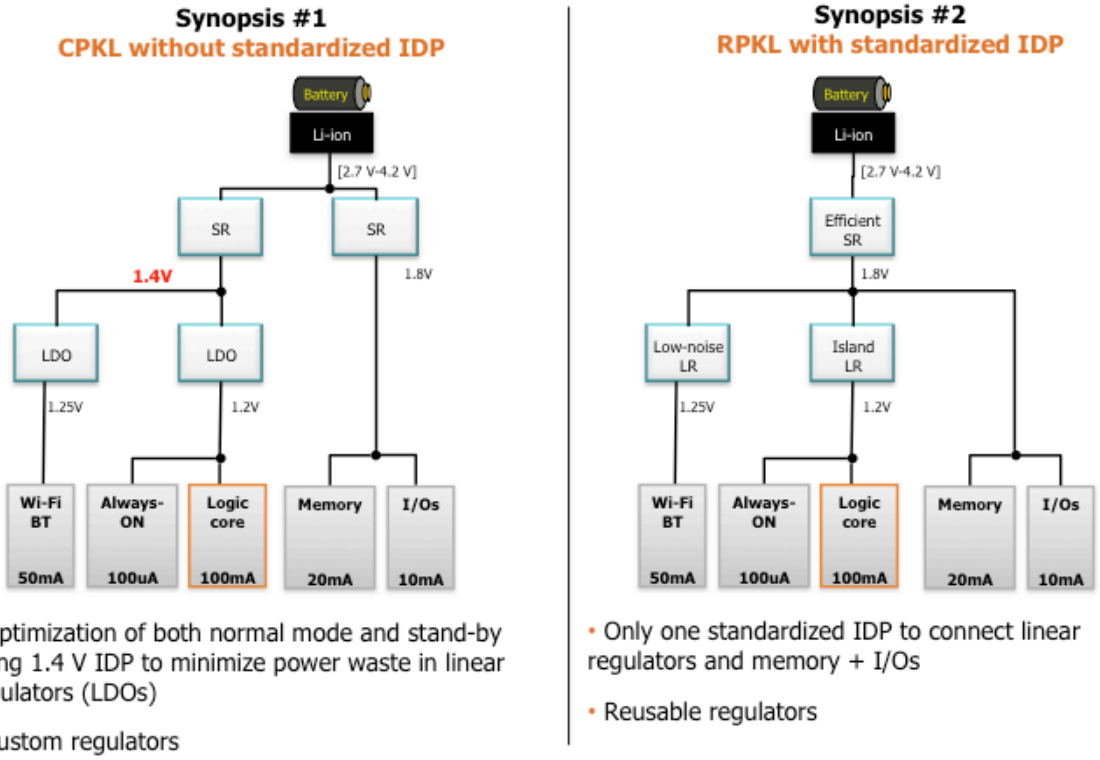

Figure 3: Comparison of PMNet architecture with and without standardized IDP

Table 1 summarizes the different performances of the two synopses in terms of BoM, silicon area, power consumption and the FoM value.

Synopsis	Approach	# of Capa-citors	# of Induc-tance	# of package pins	Normal mode consumption (mW)	Standby mode consumption (mW)	Average Power Consumption (mW)	Silicon Area (mm^2)	FoM (mW*mm^2)
#1	CPKL without standardize IDP	4	2	14	330.175	0.175	3.475	1.908	6.63
#2	RPKL with standardized IDP	3	1	10	405.225	0.225	4.275	1.204	5.15

Table 1: FoM comparison of the 2 different synopses

Thanks to the FoM, and using standardized IDP, we can see that the RPKL approach enables the best trade-off between different optimization criteria (power consumption, area) and achieves a better overall optimization (FoM). As compared to the CPKL solution, the RPKL solution represents a considerable area decrease. The CPKL solution reaches the best power consumption optimization. At application level, one additional inductor is also required impacting both BoM and PCB area (number of components and package pin counts), which are not considered in the FoM here. For this last criteria, the RPKL approach achieves also the best result.

This example illustrates the relevance and advantage of the RPKL solution at SoC level thanks to the defined IDPs, per application requirement, and the importance to consider multiple criteria at once when optimizing a PMNet.

Accuracy budgeting thanks to standardized IDP voltage range

Like for standard cell libraries, the IDPs are defined with an accuracy range of 10 %. While it may seem trivial, this 10 % accuracy range allows the budgeting of:

- Standard "DC accuracy" of 3 % at regulator output voltage, taking into account the Process, Voltage and Temperature (PVT) variations as well as the load regulation and line regulation.
- Standard "Mode Transition (MT) accuracy" of 4 %, including the disturbance due to load transient and output ripple.
- Standard "minimum IR drop" of 3 % for SoC integration budgeting:
    - In general, the regulator minimum drop-out voltage is 0.2 V.
    - When the Place and Route (P&R) is between power source and upstream regulators or between upstream and downstream regulators, the IR drop budget is at least 3 %. Depending on the current/voltage characteristics on this interface and resistive parasitics of the routing, SoC integrators now have a degree of freedom to define the acceptable routing length and width, without compromising the final system performances.

Major breakthroughs from this budgeting are:

- Standard DC and MT accuracies facilitate the combination of the proposed upstream and downstream regulation components with in-house or third party regulation components and/or loads that can be internal or external to the SoC.
- Standard allowance for IR-drop budget reduces the iterations between front-end design and back-end P&R.

Complete Power Management Solutions with RPKL regulation components and more

Based on the RPKL approach, Dolphin Integration launch the DELTA regulation component library composed of battery management components, switching regulators and linear regulators as shown in Figure 4. For each regulation component, the needed advanced views (simulation models) are provided for system-level verifications in order to minimize the risks of performance drops due to SoC operating mode transitions and different types of noise propagated through the PMNet.

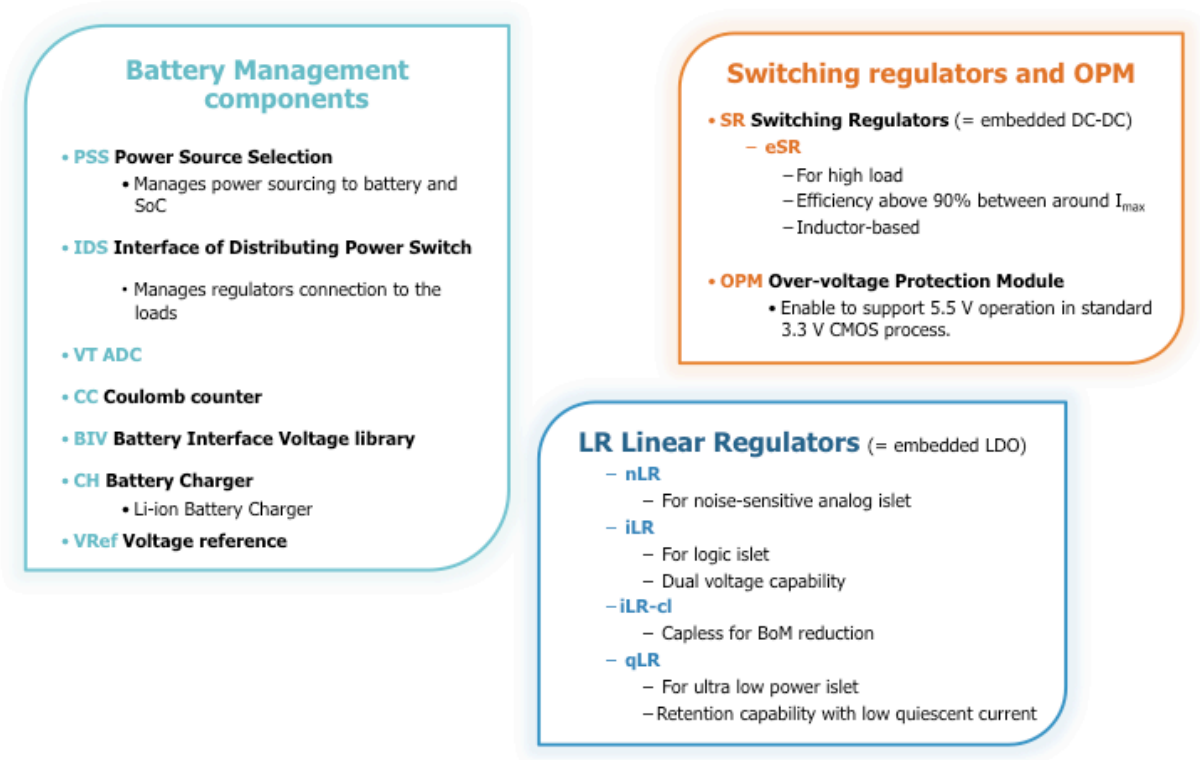

Figure 4: DELTA regulation component offering

In addition to the DELTA offering for building an optimal PMNet for reducing SoC power consumption, Dolphin Integration also provide ultra low leakage memories (divide the leakage by up to 1000) and ultra low leakage standard cell libraries (by up to 750) with direct battery connection for optimizing the SoC leakage requirement.

Win for all

This article explains the necessity and advantages of a reusable power kit approach with four pre-defined voltage levels for distributing power. These four IDPs, together with voltage accuracy, allow to set the DC accuracy of regulation components, SoC IR drop budget and AC variation tolerance due to mode transitions within the PMNet. Dolphin Integration share the seven rules (described by Figure 5), which are respected for the DELTA offering.

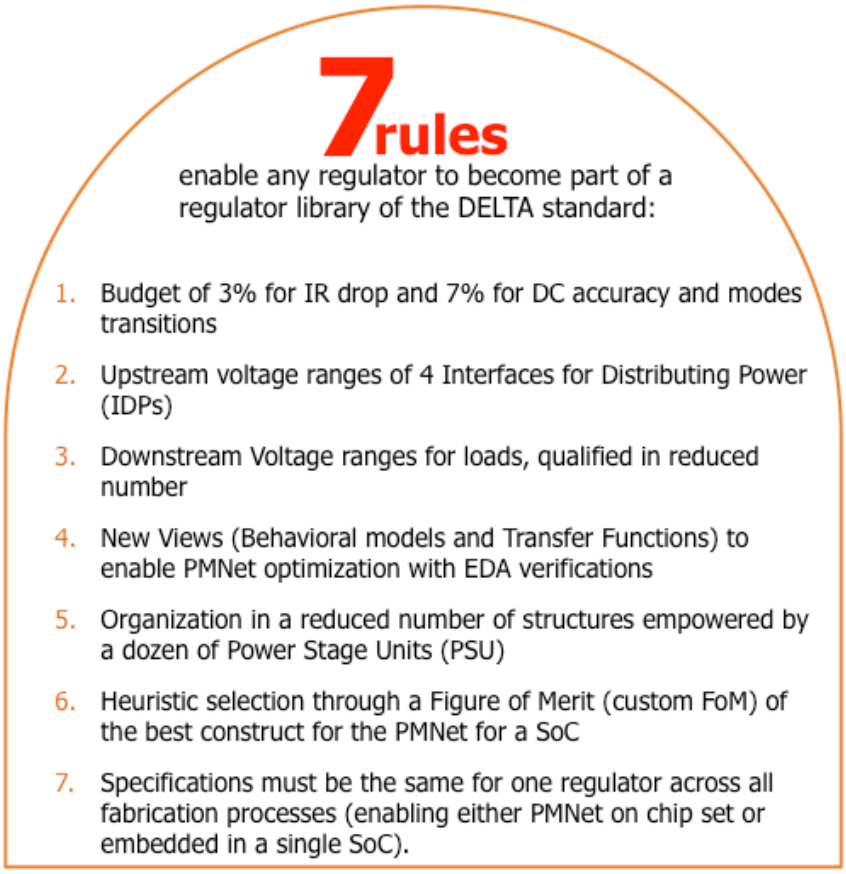

Figure 5: 7 rules of DELTA standard

Thanks to these rules, the PMNet solution leads to the fastest TTM (with reusable components), the best trade-off between different optimization criteria (thanks to FoM and standardized hierarchical assembly rules) and the best system-level risk management (with Advanced Views and EDA verifications).
By respecting these rules, any regulator can be part of the powerful PMNet solution and enjoy the benefits (summarized in Figure 6) for reaching an ultimate return on investment.

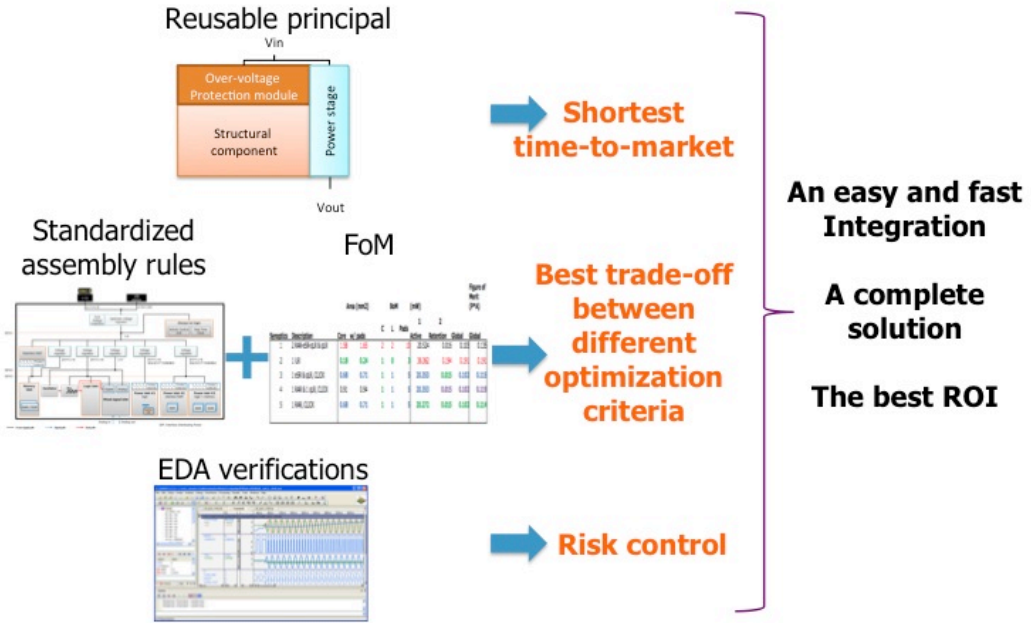

Figure 6: Complete PMNet solution

About Dolphin Integration

Dolphin Integration contribute to "enabling mixed signal Systems-on-Chip" for worldwide customers with IP components best at low-power consumption.
Their wide offering of silicon IP components is based on innovative libraries of standard cells, register files, memory generators and power regulators for flexible power supply networks. They provide power optimized micro-controllers from 8 to 32 bits, and high-resolution converters for audio and measurement applications.
Their 30 years of diverse experiences in the integration of IP components and providing services for ASIC/SoC design and fabrication, with their own solutions for missing EDA, make them a genuine one-stop shop covering all customers' needs for specific requests.
Their drive to incessantly innovate for their customers' success has led to two strong differentiators:

- state-of-the-art "configured subsystems" for high-performance applications securing the most competitive SoC architectural solutions,

a team of Central and Field Application Engineers supporting each user's need for optimal application schematics, demonstrated through EDA solutions enabling early performance assessments.

About the Author

Hugo KUO is Dolphin's FAE in mixed-signal high-resolution converter subsystem since January 2006. He co-authored several publications for launching Dolphin's worldwide strategy of Application Hardware Modeling (AHM) since 2009. He received a microelectronic engineering master degree from Grenoble Institute of Technology (INPG) in France in 2005 and is completing a part-time MBA program from HEC Paris. Mr. Kuo can be reached at fae.asia@dolphin.fr.