Accelerating Mixed Signal System Design Verification using New Diagnostic Method

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Abstract

The mixed-signal simulation of complete systems, i.e. the electronics with its attached peripherals, such as sensors and actuators, already has a firm place in today's design process. While the verification of the digital part, mostly implemented in Verilog and VHDL, has gained a speed increase through the use of Accellera's Property Specification Language PSL, the analog part suffers from not being supported by this language. To speed up the verification of the analog part (ABCD, C, SPICE, Verilog-A(MS), VHDL-AMS) a new methodology is needed. This paper presents enhancements to the PSL methodology for the application to mixed signal circuit design which commonly make use of mixed language for modeling. As demonstrator for this adapted methodology, we use a simple control circuit of a stepper motor to show the aspects of mixed-signal, multi-language and multi-domain.

Key words: mixed-signal design, verification, Detectors, specification, assertion

1 Introduction

Verification of digital hardware designs with the standardized Property Specification Language (PSL, IEEE 1850) is widely spread nowadays in HDL development design flows. Here, the PSL language is included as comments in VHDL and Verilog models source code. With this information, dedicated specification rule checks can be performed during simulation. The PSL language is restricted to event driven aspects.

However, the opportunities to integrate more and more functionality into a (micro) System-on-Chip (SoC) heavily call for advanced mechanisms in the verification of complete system simulations, i.e. to additionally take into account analog and mixed-signal aspects. This paper describes a new methodology to automatically check complete mixed-signal designs using a library of Detectors implemented in VHDL-AMS.

Chapter "The Detector Methodology" describes the new methodology. In chapter "The Demonstrator", the application of the methodology is presented. In chapter "Conclusion", we summarize the advantages of the proposed methodology for mixed signal circuit design. And in chapter "Outlook", we present in which fields the Detector methodology could bring benefits to the user.

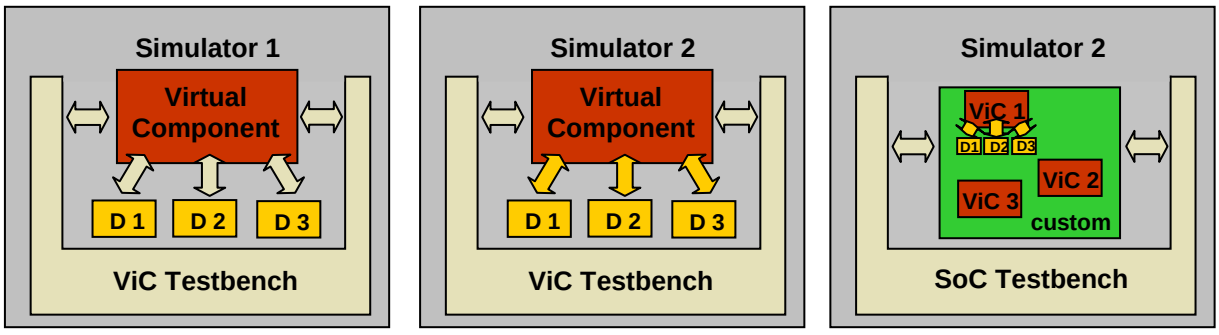
2 The Detector Methodology[1]

The Detectors are built to observe specific system characteristics, e.g. to measure currents, voltages, frequencies, slopes, delays, jitters etc., on the condition not to influence the system behavior in the simulation. So the Detectors are passive "observers" with respect to the circuit. But they are active in respect to the user: the Detectors announce online, during simulation, when signals validate specification rules and write these events in report files for further analysis. Depending on the severity level setup of the alerts, the simulation can be aborted, paused or continued.

While implementing the Detectors, special focus was set on being compatible with any possible applications, for instance through parameterization in order to be adaptable to different specifications.

Besides the analog ports for attaching the Detectors to the circuit nets to be observed, every Detector has a logic input-port to attach an enable signal and a logic output-port to supply a trigger signal to the system. So, the user is able to build more complex specification rule checkers with help of the basic Detectors already defined in the library.

The standardized hardware description language VHDL-AMS was chosen to build the library of Detectors. This ensures that designers using diverse simulators supporting mixed language (Verilog(-AMS), VHDL(-AMS), SPICE...) can benefit from these developments.



Circuit Development
Virtual Component Developer provides Virtual Component (ViC) + Detectors + Testbench reduced thanks to detectors

Circuit Transfer
The reduced Testbench must be adapted to the target simulator; the detectors remain untouched

SoC Integration
Customer integrates different ViCs together with custom circuitry into a SoC. The detectors observe the compliance of the specifications in the changed environment.

Figure 1 : Detector featured Mixed Signal Design and Circuit Transfer

Figure 1 illustrates the application of the Detectors in circuit design, transfer and SoC Integration. For Circuit design, they are helpful in speeding up the verification process through automatic specification rule checks. The detectors replace testbench specific code (possibly simulator specific) with independent detectors embedded in the overall testbench.

[1] The Detector methodology described in the following were developed and partly co-financed in the frame of the EU supported, regional funded project EMSIG (Development and transfer platform for the industrialization of mixed-signal circuits, FKZ 005-0604-0020). European Funds for Regional and Structural Development, regional project Ziel 2 Gebiet

Thanks to the use of VHDL-AMS, the same detectors can operate in different simulator environments so that they can be delivered to a customer to check if the component behaves as expected in they changed environment. For SoC Integration, Detectors enable checking that component integration rules are respected, verifying that specifications are met and detecting unexpected component interactions when integrated in a complex SoC. The main benefit is that SoC Integrators do not have to study a written specification. All the specification rules that are represented by the detectors are checked automatically during the simulation.

The advantage of using a library of Detectors, rather than of using a special language, is that already verified model libraries remain untouched. The Detectors can easily be placed inside the schematics and of course compounded specification rule checkers can be reused independently from any model.

3 The Demonstrator

The demonstrator system is a stepper motor control system. It consists of a dc voltage power supply, two H-bridges, a control unit to drive these bridges, an H-bridge power electronic part per phase and a 2-phase stepper motor. Additionally, different instances of Detectors are placed for current specification observing.

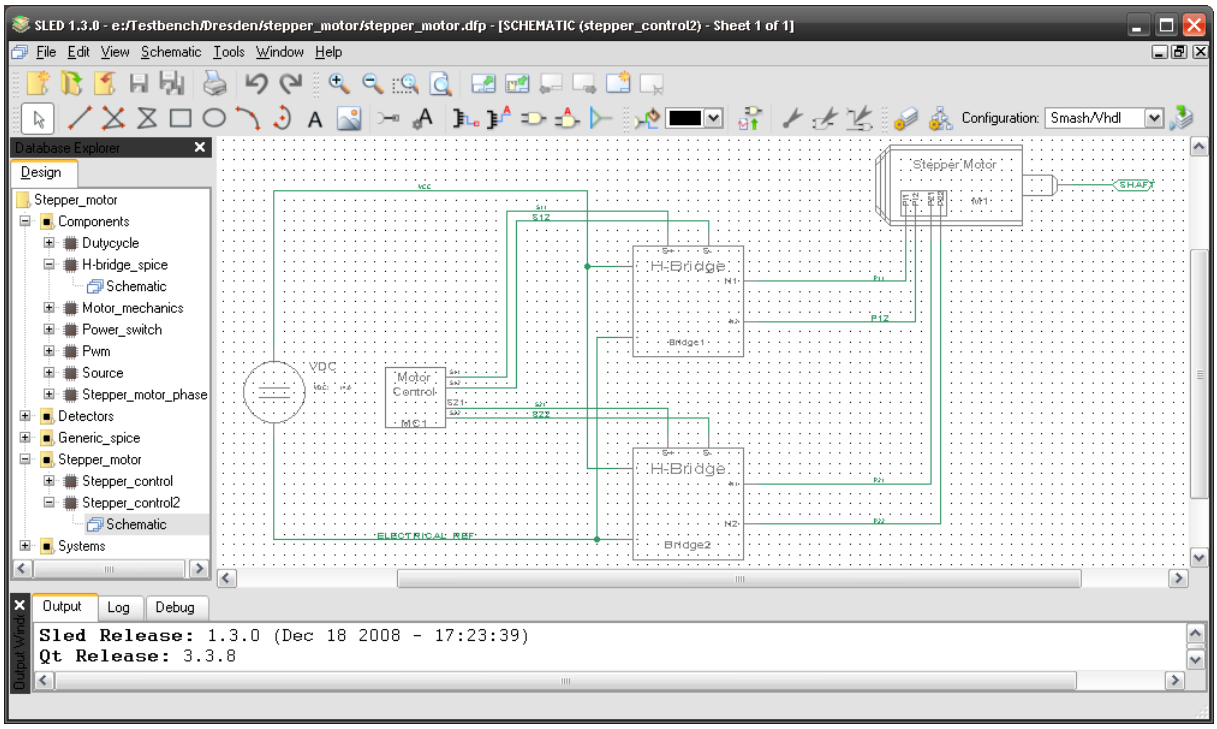


Figure 2: Complete stepper motor system circuit

Figure 2 shows the top level schematic of the system in the schematic editor SLED[2]. The stepper motor models and the control circuit are part of the freely available VDA[3] VHDL-

[2] **S**chematic **L**ink **ED**itor, EDA tool of Dolphin Integration http://www.dolphin-integration.com
[3] VDA: Verband der Automobilindustrie http://www.vda.de/

AMS model library[4]. This library has been set up in frame of the work in the FAT-AK30[5] group. Slight modifications were necessary at the control circuit in order to drive the H-bridges. Beside the Detectors, the stepper motor and the voltage source are implemented in VHDL-AMS, whereas the power electronics parts, the H-bridges, are implemented in SPICE.

The application of the new methodology is demonstrated by checking if the power electronics part is correctly dimensioned, i.e. if the currents through the stepper motor phases don't exceed the H-bridge transistor specifications.

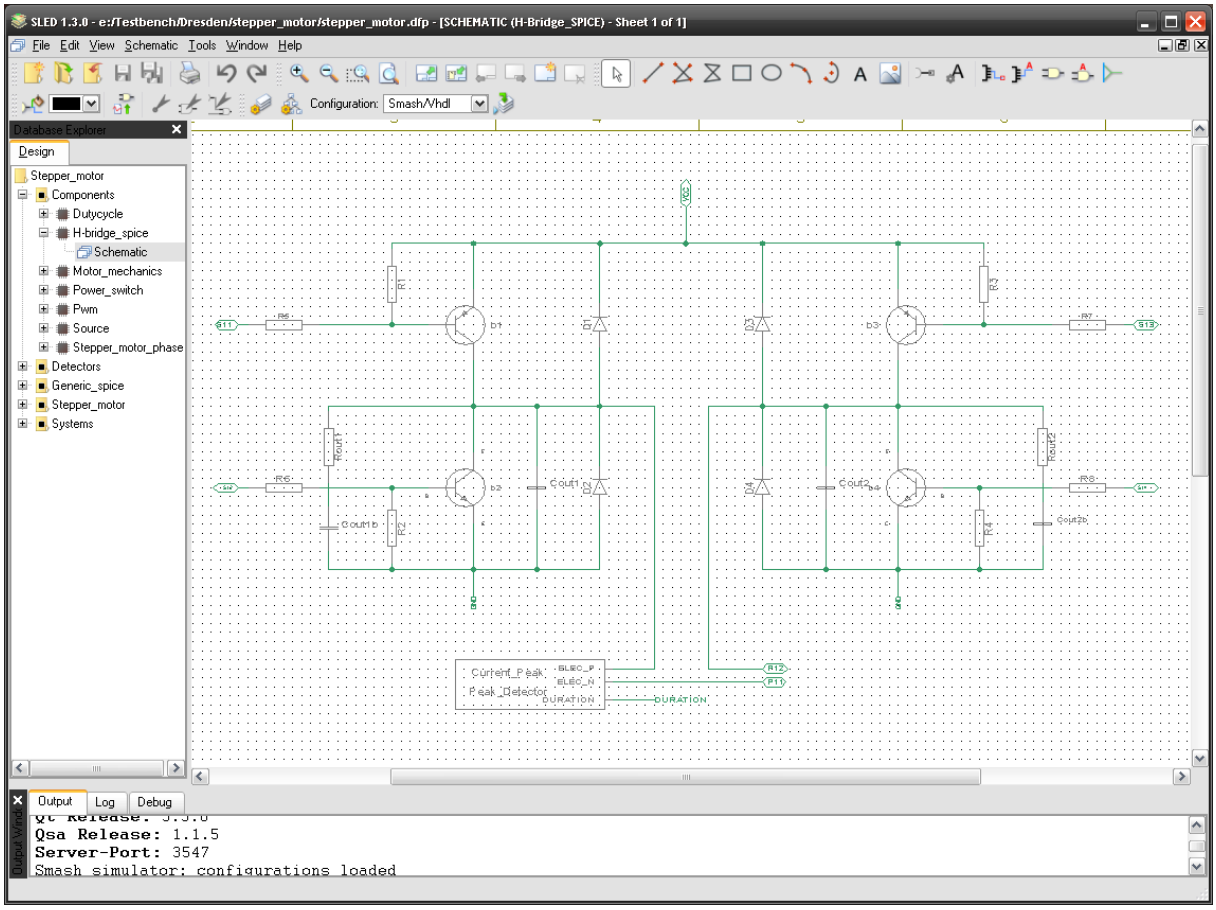


Figure 3: Sub-circuit of the H-bridge including compounded current Detector

Figure 3 shows the power electronics sub-circuit, the H-bridge, with an instance of a current Detector sub-circuit. This sub-circuit observes if the current through the H-bridge transistors doesn't exceed their specifications of 8A operating current and 15A peak current, with a maximum peak duration of 300µs. Figure 4 shows the Detector sub-circuit.

[4] Model library download: http://fat-ak30.eas.iis.fraunhofer.de/mb/index_en.html
[5] FAT: Forschungsvereinigung Automobiltechnik e.V. - Arbeitskreis 30 "Simulation gemischter Systeme" http://www.vda.de/de/verband/fachabteilungen/fat/

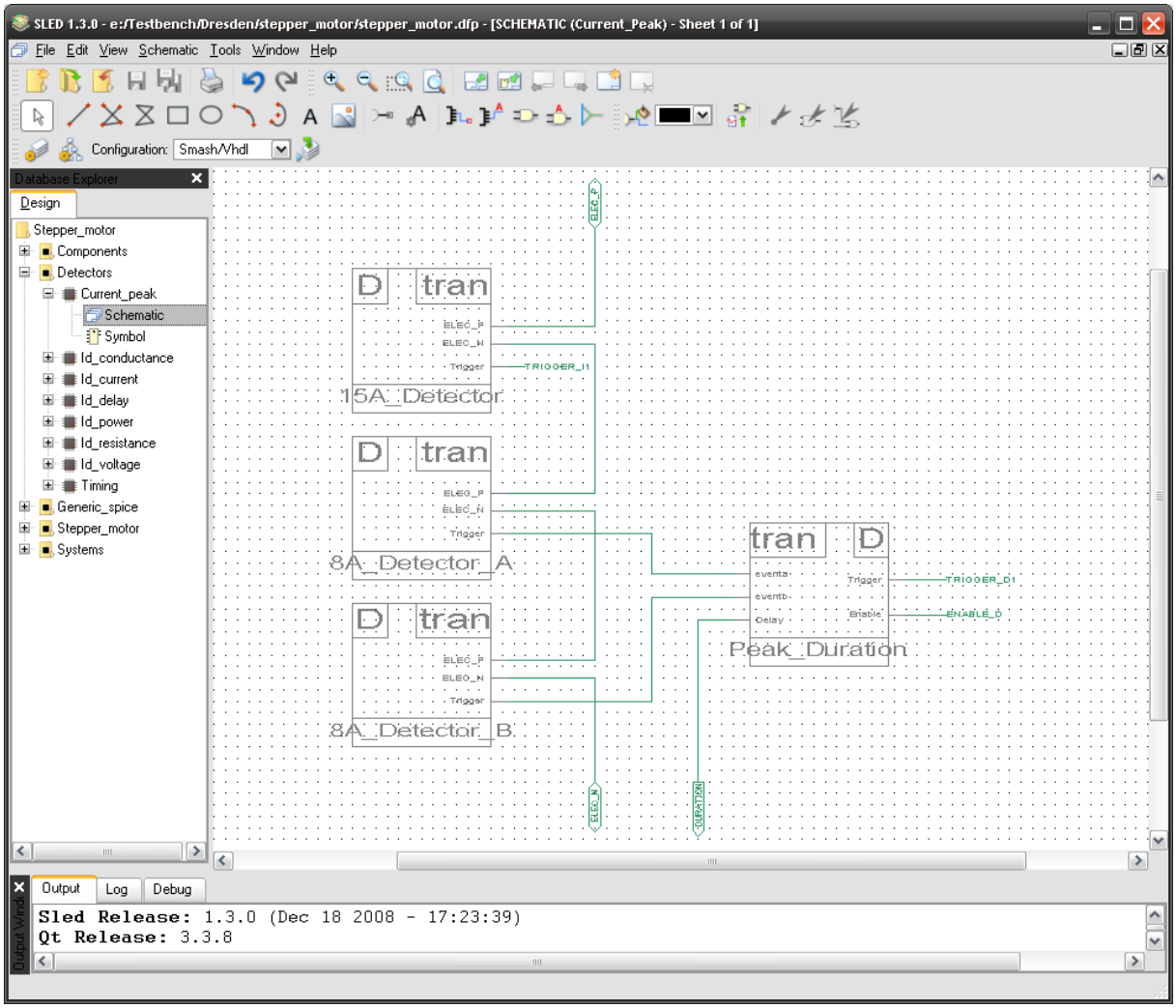


Figure 4: Sub-circuit of the compounded current Detector

The Detector measures the current output of the H-bridge, i.e. the current through a stepper motor phase. One current Detector (15A_Peak_Detector) observes if the current exceeds the maximum peak current specification of 15A. The other current Detectors observe if the current exceed the maximum allowed operating current of 8A, whereby Detector (8A_Detector_A) detects if the current is higher than 8A and then starts the time measurement of the duration Detector. The last current Detector (8A_Detector_B) stops the time measurement when the current goes below 8A, i.e. the combination of the current detectors together with a duration Detector (Peak_Duration) measures the duration of the current peak. When the current exceeds 8A, which is the maximum current for the TIP 102 and TIP 107 transistors, the issue is immediately displayed in the simulator SMASH[6], see Figure 5.

The first trace in the Figure 5 shows the rotor position, the second trace displays the current through motor phase 1 and the third trace visualizes the current through motor phase 2. The window in the foreground shows the warnings when the current crosses the 8A limit. The notes record when the current goes below the specification limit of 8A again. The simulation time is logged together with the events. Beside the display in the window, the

[6] Single kernel, mixed-signal, multi-level, multi-domain simulator by Dolphin Integration

events are written in a log-file for later off-line analysis, see Listing 1 for the 8A Detector report and Listing 2 for the Motor phase 1 peak current duration Detector log-file.

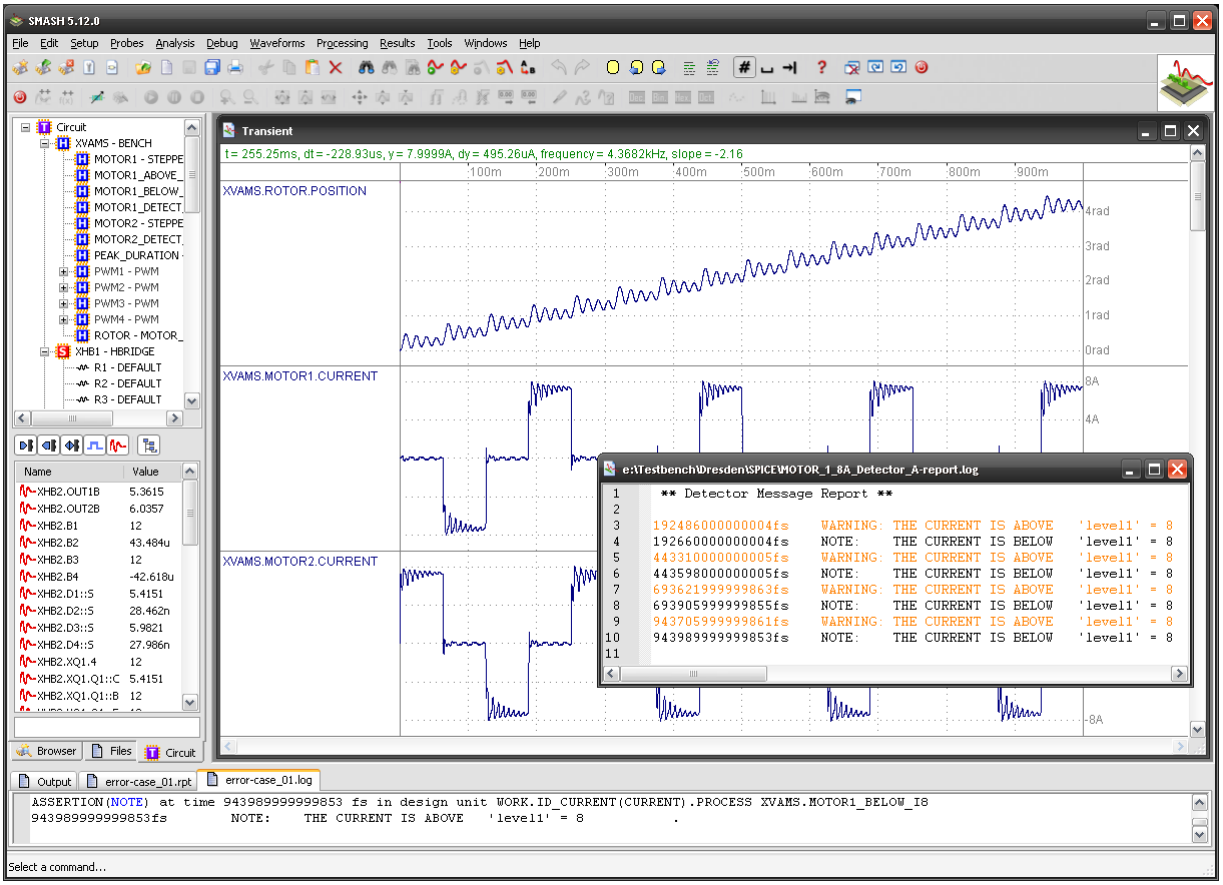


Figure 5: Simulation of the stepper system, showing current Detector warnings

```
** Detector Message Report **
192486000000004fs  WARNING: THE CURRENT IS ABOVE       'level1' = 8
192660000000004fs  NOTE:    THE CURRENT IS BELOW       'level1' = 8
443310000000005fs  WARNING: THE CURRENT IS ABOVE       'level1' = 8
443598000000005fs  NOTE:    THE CURRENT IS BELOW       'level1' = 8
693621999999863fs  WARNING: THE CURRENT IS ABOVE       'level1' = 8
693905999999855fs  NOTE:    THE CURRENT IS BELOW       'level1' = 8
943705999999861fs  WARNING: THE CURRENT IS ABOVE       'level1' = 8
943989999999853fs  NOTE:    THE CURRENT IS BELOW       'level1' = 8
```

Listing 1: Motor phase 1 current Detector log-file

```
** Detector Message Report **
192486000000004fs  NOTE:      Peak duration 174000000000 fs
443310000000005fs  NOTE:      Peak duration 288000000000 fs
693621999999863fs  NOTE:      Peak duration 283999999992 fs
943705999999861fs  NOTE:      Peak duration 283999999992 fs
```

Listing 2: Motor phase 1 peak current duration Detector log-file

Also the log-files show what has been presented by the simulator: the current is only a short time over the limit of 8A, which is the maximum continuous current for the transistors. Since the duration of the peak does not exceed the specification only a warning is shown. The maximum allowed pulse current is 15A, ≤300µs.

With the information from the basic current detector and the compounded peak current detector, the designer can easily see that the specification is not exceeded.

4 Conclusion

It has been shown that with the use of the proposed methodology, the designer is able to create specification rule checkers by using and combining the parameterized Detector elements. During simulation, the detectors check whether the circuit operates in its specification and raises exceptions otherwise. Consequently, the verification phase can be automated which avoids error prone manual analysis of signal traces. All this increases designer's productivity and ensures design security through an accelerated automatic check and report of important events. Since the Detectors are implemented in a standardized HDL, they guarantee the compatibility of separate application schematics and different simulators and minimize efforts in creating and embedding specification rule checks independently of the overall testbench.

5 Outlook

The Detectors offer diagnostic support in several steps:

- Mixed-signal Circuit Design
  - Place Detectors at internal nets to observe specification violations
- (Multi Level) Model Calibration
  - Use a sequencing method to adapt model parameters to converge to measurements or simulations on lower levels.
- Circuit Optimization
  - Use a sequencing method to optimize circuit parameters
- Design Robustness Tests
  - Use a sequencing method to ensure that the IP stays in its specification
- Circuit Transfer
  - Provide virtual sockets with Detectors on IP’s ports to observe specifications of IP independently from HDL/Simulator
- Equivalence check
  - Provides possibility to check the equivalence between:
    - Two models of the same or different level of abstraction
    - Two models of the same or different language
    - A model of any abstraction level (and language) and measurements

Literature

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[4] Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme IMS – Duisburg: Final Report on Library Development, 2008

[5] Fairchild Semiconductor data-sheet: TIP100/TIP101/TIP102 NPN Epitaxial Silicon Darlington Transistor

[6] Fairchild Semiconductor data-sheet: TIP105/TIP106/TIP107 PNP Epitaxial Silicon Darlington Transistor