DOLPHIN INTEGRATION

STANDARD CELL LIBRARIES FOR ALWAYS-ON POWER DOMAIN

Introduction

Standard-cell library offering is usually divided in three categories: 6/7-track library for cost driven requirements, 8/9-track library for mainstream requirements and 10/12-track library for high-speed requirements. Standard cell Libraries often includes Multi Vt / Multi-channel-length cells to provide further flexibility to achieve the best PPA trade-offs.

However, the advent of battery-operated devices, which spend most of their time in a sleep mode, translates into an emerging need for standard-cell libraries specifically optimized for addressing the challenge of always-on power domain. Indeed, the always-on domain, typically including a logic block that remains active in all operating modes, must satisfy specific requirements in terms of operating voltage range and power consumption targets that may not be efficiently addressed by a conventional standard cell library.

The comparative analysis of the contents of three always-on power domains, as typically seen with SoCs targeting Wearables applications, enables to identify the characteristics of the standard-cell library required to reach the targeted key performance indicators.

This technical paper illustrates, with concrete examples based on 55 nm uLP-eFlash process, the various choices which may guide the SoC designer to select the most suitable standard-cell library for implementing the always-on logic among:

- Conventional high-density logic library, operating at core transistor voltage (such as SESAME uHD or HD library).
- Logic library operating at ultra-low voltage (such as SESAME NTV library).
- Logic library with extended operating voltage range (such as SESAME BiV library)

This article concludes with recommendations for selecting consistently the other silicon IPs needed for designing the always-on domain.

Always-on power domain

The Always-On (AON) power domain is the first part of the circuit supplied at power-up. It manages the boot sequence, and it remains powered whatever the operating mode, until the whole system is completely shut-down. This power domain handles the activity monitoring to wake-up the SoC whenever needed, the sequencing and management of clock and power supply during first start-up and at any power mode change (i.e. enter/exit from a "sleep" mode).

The logic blocks of the AON power domain ("always-on logic") typically consists in a power management controller (to turn on and off the power domains of the SoC) and some logic wake-up triggers to recover from sleep mode and to resume normal operation.

The logic triggers embedded in the Always-On power domain are specific to the application requirements: e.g. a Real-time Clock (RTC) associated with a 32 kHz oscillator (XTAL or RC),

a voice activity detection trigger possibly associated with a faster clock (a few MHz) and some digital IO pads to connect a microphone, etc.

If some application data needs to be preserved in "sleep" modes, the Always-On domain may also include a mean (retention RAM, retention registers, or always-on registers) to save/restore these data.

Comparative analysis between three types of standard-cell libraries

Three types of standard cell library for implementing logic of the always-on power domain are considered for the comparison.

Library type	Description
Conventional high-density standard-cell library	Typically based on 6 or 7 tracks, optimized for high-density, using HVT devices (if this layer is available) and supplied at nominal voltage. Reference in Dolphin integration catalog: SESAME HD & SESAME uHD
Standard-cell library optimized to operate at ultra-low voltage	Library specifically designed with core transistors to operate safely Near Threshold Voltage with a reasonable speed degradation to support speed requirements of an Always-on logic. Reference in Dolphin integration catalog: SESAME NTV
Standard-cell library supporting extended operating voltage range	Implemented with thick-gate-oxide transistors, the advantage is twofold: an extended voltage range enables a direct connection to the battery (if not higher than 3.6 V), thus avoiding the need for any voltage regulator, and thick gate-oxide transistors leak significantly less than core transistors. Reference in Dolphin integration catalog: SESAME BIV

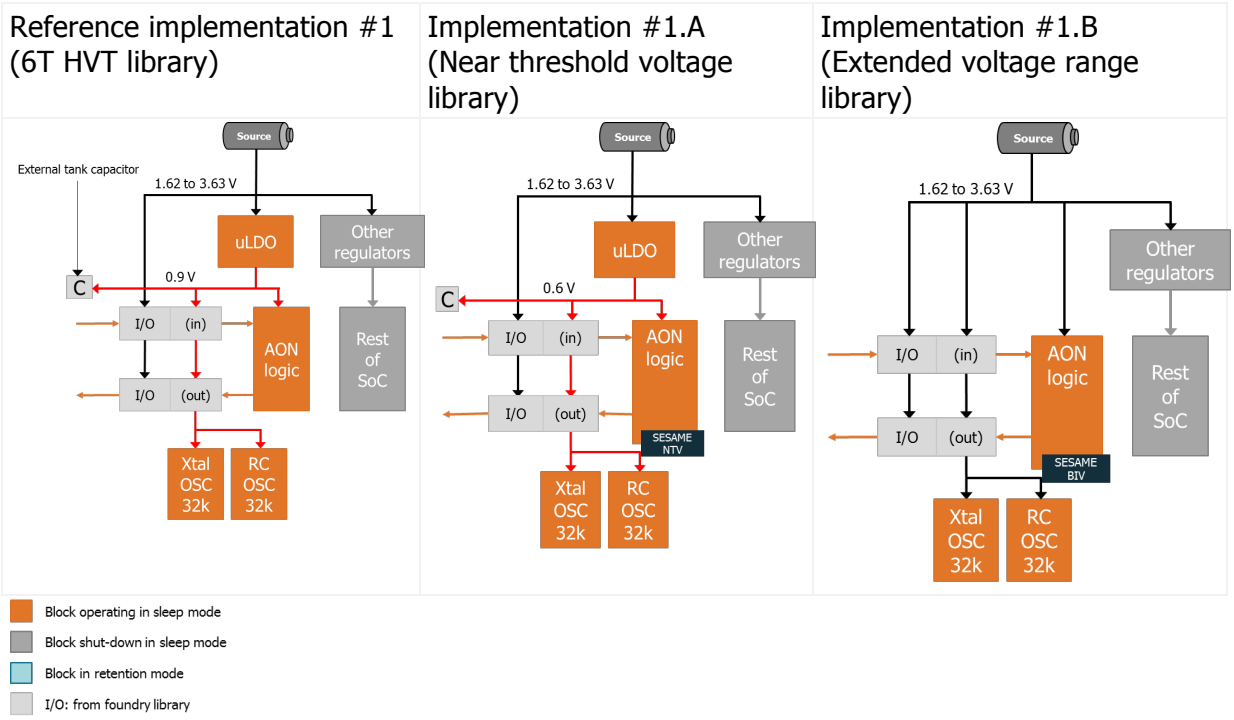
Three configurations of an always-on power domain

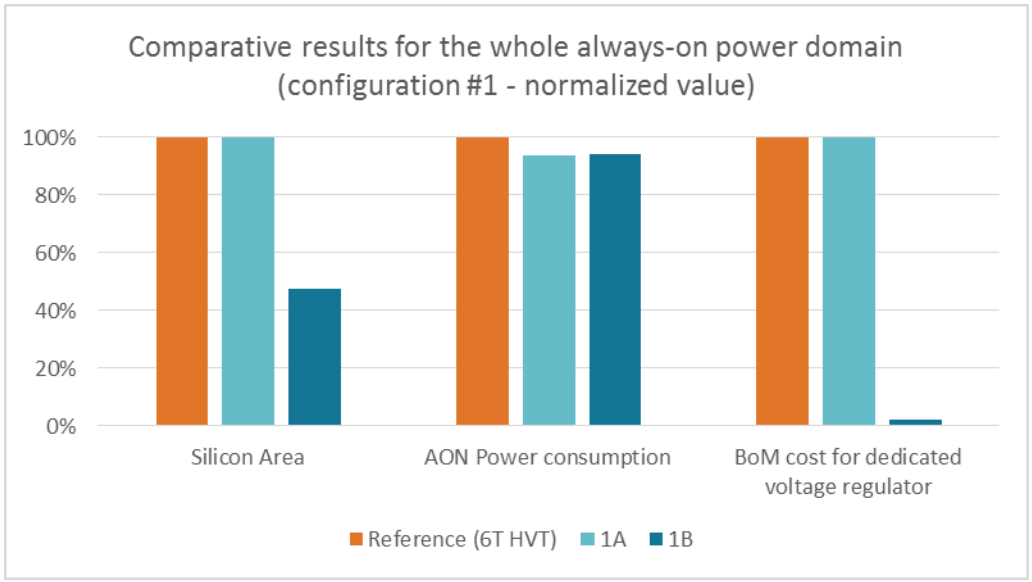
The contents of three typical configurations of an always-on domain – which are representative of a wide range of low-power SoC - have been analyzed to identify the characteristics of standard-cell library which provide the best outcome.

Configuration #1: embedding a RTC only

This configuration of the always-on domain is based a logic block (5 kgates @ 32 kHz) embedding an RTC and the PMU logic/ACU, two 32 kHz oscillators and some IOs to receive and acknowledge external wake-up events. Three assumptions are made:

- This always-on power domain has an independent supply from the rest of SoC. The rest of SoC is supplied by dedicated voltage regulator(s)
- The maximum input voltage does not exceed the maximum voltage supported by 3.3 V thick oxide transistors.
- All the blocks needed for the always-on power domain support the same voltage range as the standard-cell library.





Conclusion:

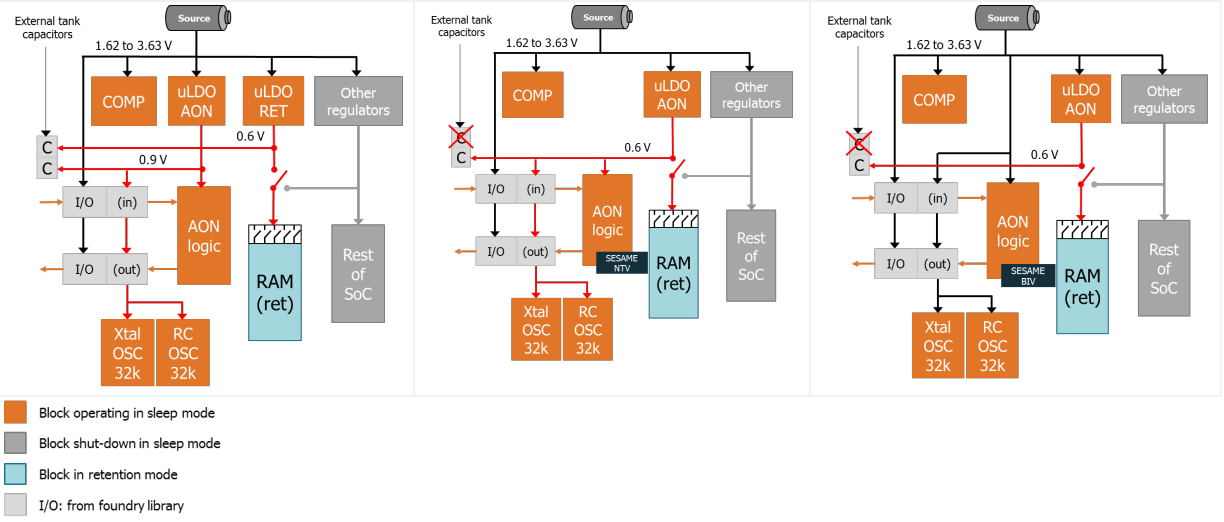
From a power consumption perspective, the always-on power domain designed to operate at Near Threshold Voltage (config. 1A) is the best but without any significant advantage. For such a configuration of the always-on power domain, the optimal solution is to rely on a library supporting an extended voltage range (thick gate oxide library) as it enables to save silicon area and BoM cost (pin + external capacitor).

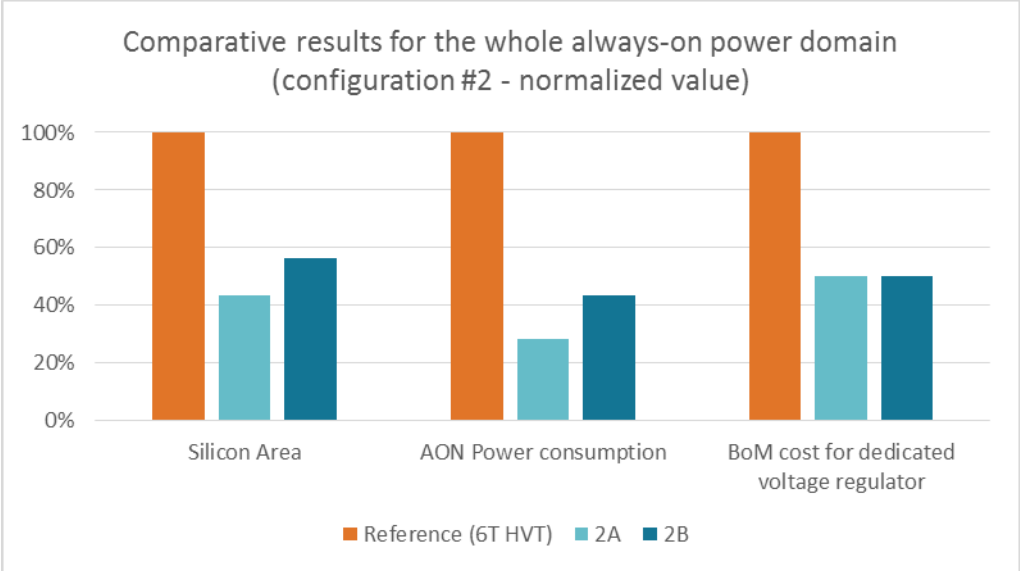
Configuration #2: RTC + voltage comparator + memory in retention

This implementation of the Always-on power domain corresponds to configuration #1 enriched with an analog comparator to generate wake-up events from an analog signal, and with 2 kB SRAM in retention at 0.6 V (lowest retention voltage).

An additional assumption is made: The memory has two possible supply sources depending on its power mode.

Reference implementation #2 (6T HVT library)	Implementation #2.A (Near threshold voltage library)	Implementation #2.B (Extended voltage range library)





Conclusion:

The implementation Solution 2A provides the best performance in all three dimensions considered: area, power saving and BoM cost. It indeed enables to eliminate a voltage regulator compared to a traditional approach. Furthermore, the capability to operate the always-on power domain at the same voltage as the RAM retention voltage translates into significant power saving: the current draw at very low voltage is much lower for the RAM and for the digital logic block.

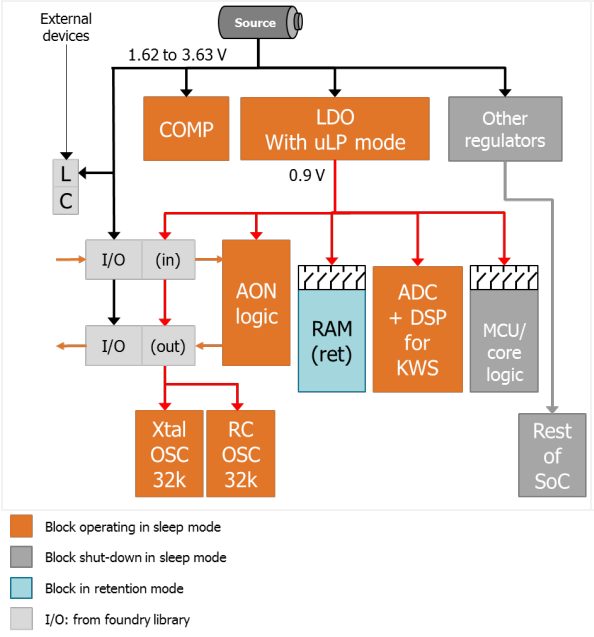
Configuration #3: RTC + voltage comparator + memory in retention + voice trigger + same supply rail

This implementation of the always-on power domain corresponds to configuration #2 enriched with a detection of voice activity (ADC+DSP for Key Word Spotting) capable of operating at high frequency when needed (e.g. 12 MHz) in normal mode.

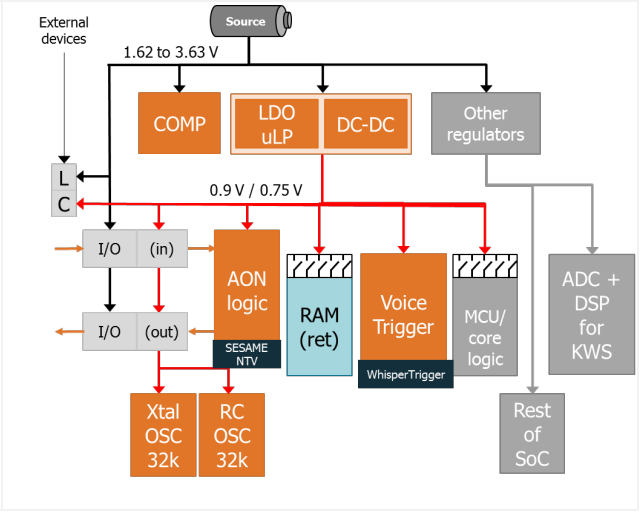
A new assumption is made: this always-on power domain is supplied using the same voltage rail as the rest of core logic.

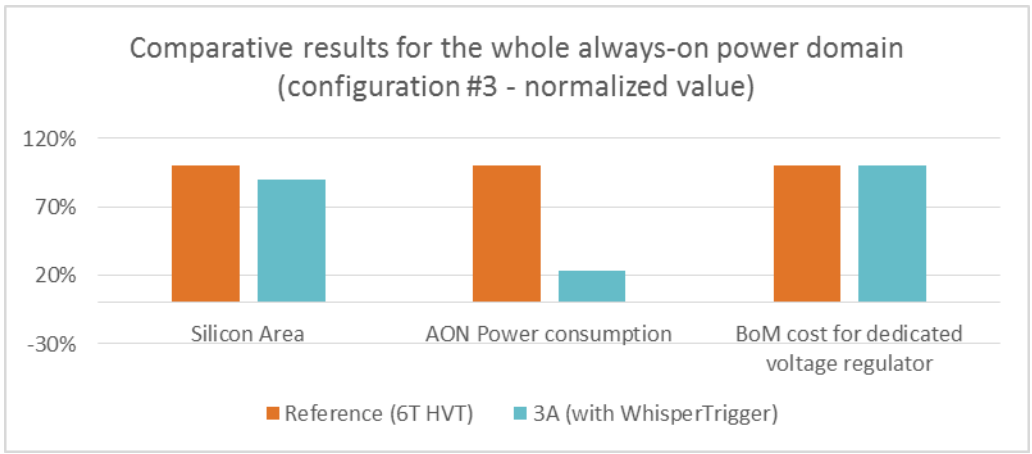
Important note: An implementation using an extended voltage range library does not make sense with such a configuration due to the high complexity of the logic that will translate into an unacceptable silicon area. Moreover, the timing constraints eliminate this option: fast operations at high voltage are definitely not appropriate to save power.

Reference implementation #3



Implementation #3.A
(Near Threshold Voltage library)





Conclusion:

The combined usage of a Near Threshold Voltage standard-cell library with the innovative Voice Activity Detector (WhisperTrigger™) enables to save significant power consumption. Using such a library is possible if it enables to operate at several MHz at low voltage (as feasible with SESAME NTV).

The use of a Voice Activity Detector enables to switch-off the audio ADC and DSP until a voice activity is detected which translates in major power consumption savings without altering the system functionality.

Conclusion

The selection of the standard-cell library for implementing the always-on logic is clearly context-dependent as demonstrated by these three configurations. The use of a thick gate oxide standard-cell library is a relevant choice for a simple configuration of the always-on power domain (RTC + small control logic) if the battery voltage is not higher than 3.6 V and as long as there is no need to retain some data in SRAM. In other cases or configurations, supplying the always-on power domain at the lowest voltage - using a Near Threshold Voltage standard-cell library – translates into the best PPA. As a general rule, whenever data must be retained in a SRAM, supplying the full always-on power domain at the same voltage as the SRAM data retention voltage is the best solution for saving power but also area and BoM costs.

Targeting to supply the always-on power domain close to the Near Threshold Voltage makes sense if the whole set of elements - such as the voltage regulators, the clock oscillators… are also designed to safely operate at such a low voltage.

To help its users achieve the best PPA targeted by next generation of battery-operated devices, Dolphin Integration proposes a complete panoply of silicon IPs for the always-on power domain. This offering combines:

- **FOUNDATION IPs** (SESAME BIV & NTV library and SpRAM Rhea with low voltage retention mode),
- **FEATURE IPs** (e.g. qOSC-XTAL low power crystal oscillator and WhisperTrigger™ Voice activity detector) and
- **SoC FABRIC IPs** (e.g. qLR ultra-low power voltage regulator and MAESTRO flexible and modular power management controller)

Dolphin Integration IPs

SESAME BiV
https://www.chipestimate.com/log.php?from=%2Fip.php%3F10%2Btrack%2Bthick%2Boxide%2Bstandard%2Bcell%2Blibrary%2Bat%2B%26id%3D40202%26partner%3DDolphin%2520Integration&logerr=1

SESAME NTV
https://www.chipestimate.com/ip.php?Near+Threshold+Voltage+standard+cell+library+at+TSMC+&id=40220&partner=Dolphin%20Integration

RAR eSR-qLR
https://www.chipestimate.com/ip.php?Retention+Alternative+Regulator,+combines+high+efficiency+in+normal+&id=40345&partner=Dolphin%20Integration

About the author

Didier Maurer
Following an engineering degree from Grenoble University, Didier Maurer joined 8/16-bit MCU design team at Dolphin Integration in 1999 as digital designer. He then took over the team leadership for 6 years before making a career move to customer support. He is now a senior FAE more specifically in charge of Foundation IPs.