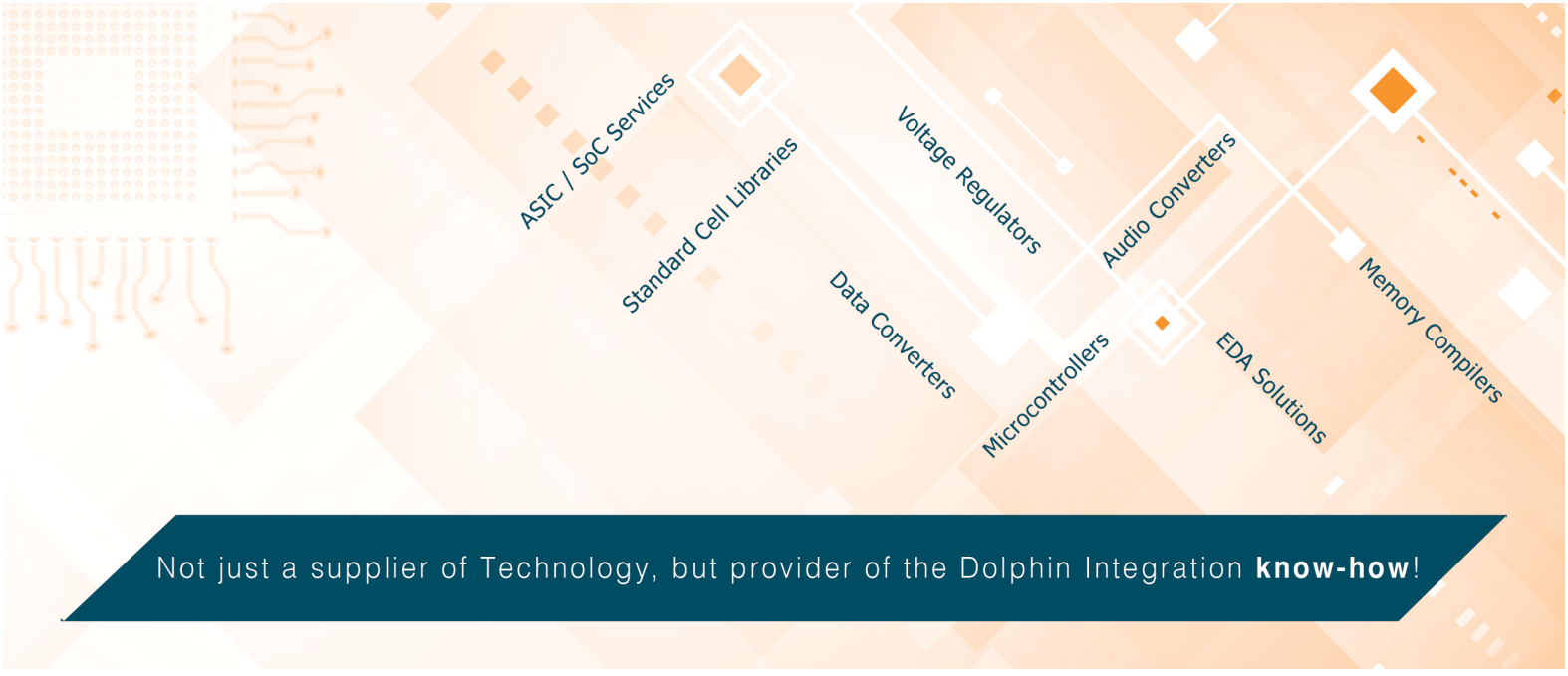
DOLPHIN INTEGRATION

CAPLESS REGULATORS – DEALING WITH LOAD TRANSIENT



1. Introduction

In the promising market of the Internet of Things (IoT), System-on-Chips (SoCs) are facing complexity challenges and stringent integration requirements. The architectural definition, component selection and their integration of the power management systems play a major role in the quest of device minimization and battery lifetime maximization. Capless voltage regulators are seen as the best answer to overcome the integration and Bill of Materials (BoM) requirements by suppressing the need of an off-chip capacitor.

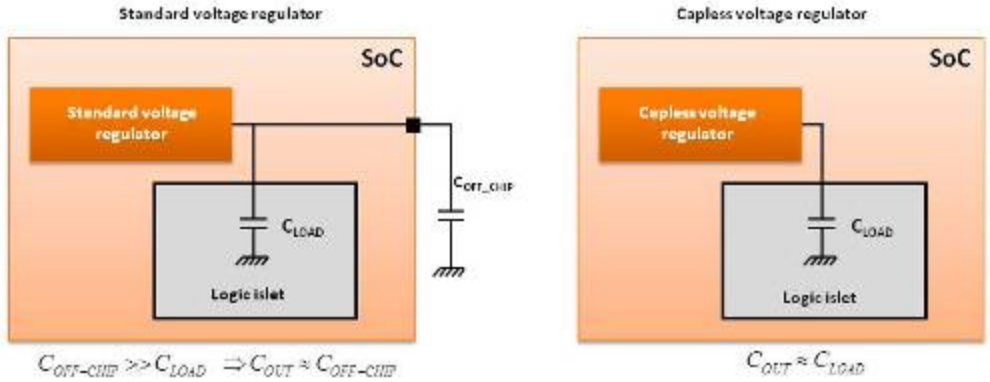


Figure 1: Standard versus capless voltage regulator synopses

2. Logic Load and Average Current

A voltage regulator must maintain the output voltage stable for any variations of the load current.

Since most regulators are not fast enough to react to each individual current pulse of a logic load, they can only supply an average current. Therefore regulators will react identically to dynamic logic load current profile as to a current step reaching the same current averaged over a clock cycle, and with rise time similar to the first pulse rise time. Charges are first drained from the internal capacitor, inducing a voltage drop, that is recovered by the regulator once its feedback loop has been readjusted.

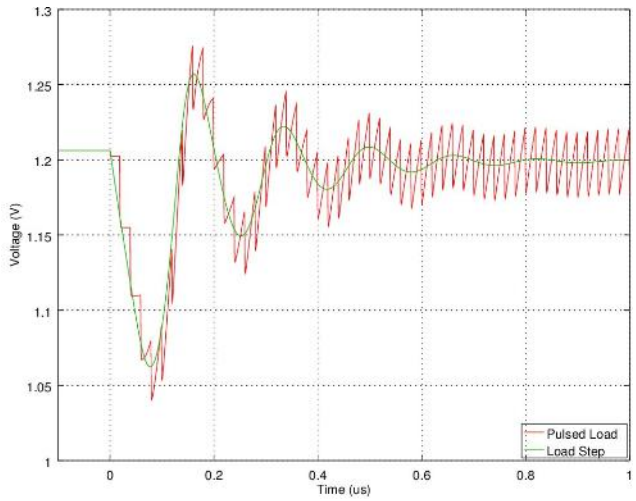


Figure 2: Regulator transient response to a pulsed load and to a corresponding load current step

Therefore internal capacitor is needed to provide charges during each event and maintain internal supply integrity. Internal capacitor must be inserted as close as possible to the load to be supplied, and additional internal capacitors must be planned to make sure dynamic voltage drops due to load activity are kept within reasonable limits. Those two capacitors, combined with the capacitance of the load, define how much capacitance the capless regulator will see on its output.

3. Load Transient and Voltage Regulator Accuracy

The load transient performance is defined as the ability of the voltage regulator to respond to a sudden change in the load current. It is generally expressed as percentage of variation with respect to the regulator output voltage.

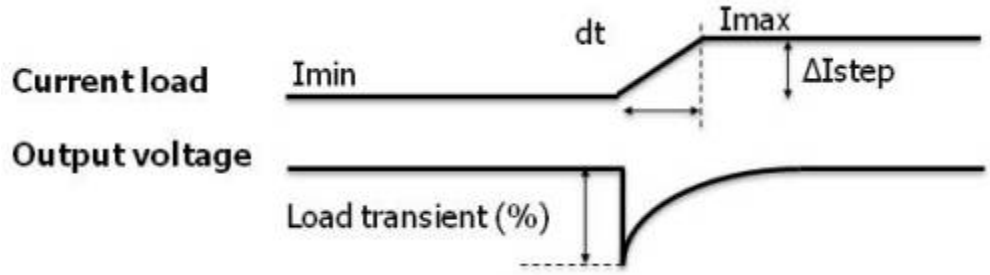


Figure 3: Load transient response definition

As the standard-cell libraries are defined with the accuracy range of ±10 %, the budget pondering between regulator accuracies and the SoC IR drop has to comply with this voltage

range, otherwise timing violations might occur or data integrity can be compromised. To ensure an achievable and not over-constrained design of both the regulator and the SoC power grid, this ±10 % accuracy range allows the following budget:

• Standard “DC accuracy” of 3 % on regulator output voltage (including the Process, Voltage and Temperature (PVT) variations as well as the load regulation and line regulation of the regulator)

• Standard “Mode Transition (MT) accuracy” of 4 % (including the disturbances due to load transient and output ripple)

• Standard “IR drop” of 3 % (including all integration parasitic — bonding, packaging, PCB, on-chip routing).

Since capless voltage regulators are linear regulators, the Mode Transition (MT) accuracy only refers to the load transient variations because they have no output ripple (in comparison to switching regulators).

Consequently, for matching with the standard cells accuracy requirement, the load transient performance of a capless voltage regulator should comply with the 4% accuracy. Otherwise, the more variation margin is used by the regulator, the less will be left for the power distribution network.

4. Capacitance Impact on the Load Transient

The voltage regulator output response to a sudden change in the load current mainly depends on the following parameters:

- The speed of the voltage regulator (GBW: Gain BandWidth product)
- The load current step (Δi) and its change rate (di/dt)
- The total capacitance on the output of the voltage regulator (Cout)

Due to its limited bandwidth (GBW), in case of fast changes of load current, the voltage regulator will not be able to provide the required instantaneous current. The output capacitor will thus provide the difference of current between the steady-state load current and the new current until the regulator can totally supply the new current value.

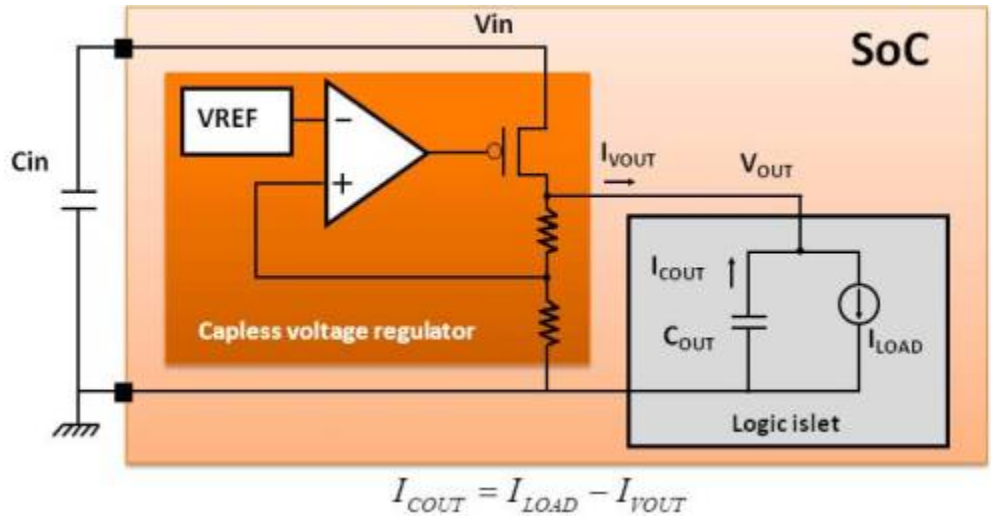


Figure 4: Basic capless voltage regulator diagram

For voltage regulators using external capacitor, the capacitance for the external passive component is generally in the range of 1 to 10 µF. This is enough to keep the output voltage within a few percent until the regulator loop readjusts. For capless regulators, the total output capacitance (Cout) is totally internal and is thus in the 100 pF to 100 nF range. At such values, the charge tank is significantly reduced and thus limits the ability to properly maintain the output voltage in case of fast load transients.

To give an order of magnitude, let's consider the voltage variation on a capacitor charged at 1 V due to current changing from 0 to 100 mA. The time required for the voltage to drop by 4 % is (respectively for a 1 µF and a 1 nF capacitors):

$$dt = \Delta V \times \frac{C_{OUT}}{I_{LOAD\_MAX}} = 4\% \times 1V \times \frac{1\mu F}{0.1A} = 400\,ns \quad (1)$$

$$dt = \Delta V \times \frac{C_{OUT}}{I_{LOAD\_MAX}} = 4\% \times 1V \times \frac{1nF}{0.1A} = 400\,ps \quad (2)$$

Thus, the capacitor can hold the output voltage within the accuracy of 4 % for 400 ns using an off-chip 1 µF capacitor, but only for 400 ps using an on-chip capacitance of 1 nF. Consequently, a capless voltage regulator with an output capacitance of 1 nF must supply the current required by the load in less than 400 ps to meet the 4 % accuracy requirement. This represents a bandwidth of about 1 GHz.

No capless regulator has such a fast response time, therefore, some adjustments must be made. For example, the on-chip decoupling capacitance might be increased by filling every possible area, this is a measure that most integrators will already take once the layout is almost done. Or, the load current might be increased in steps, by first starting the clock tree and then the logic function, or by starting the supplied modules one at a time, thereby giving time to the regulator to supply enough current before demanding more.

5. Load Transient for Capless Regulators

For voltage regulators with an off-chip capacitor, the load transient performance is generally quite easy to define since the external capacitor allows to sustain fast and significant current transitions.

Generally, load transient performance of regulators using an off-chip capacitor is defined only for a typical load current change, with some specified ramp time between 50 ns and a few microseconds. The ramp time is indicative of the impact of parasitics (bonding, package, PCB) delaying the supply of charges from the external capacitor to the internal circuits. Therefore, the regulator will see a current that changes gradually. For instance, one typically sees "Load transient, from 1 to 100 mA in 1 µs = 100 mV" in specifications.

Load transient performance of a capless regulator is more difficult to define as sudden current changes must be managed by the voltage regulator and the smaller on-chip capacitor.

A capless regulator will only see the average current of the load as for regulators using an off-chip capacitor, but the parasitics between the regulator output and the load are much smaller in this case. Therefore, the regulator output will see the current change occurring much faster (~100 ps) for logic loads, the actual value depending on the process node and the integration. Analog load current might ramp much more slowly depending on its nature.

To properly specify the load transient of a capless voltage regulator, both the total load capacitance and the load-current step must be considered.

In order to achieve the appropriate voltage transient performance, Dolphin Integration features the Load Current Tolerance Abacus (LCTA) in the ViC Specification of capless voltage regulators. The LCTA informs about the maximum drop in percent of voltage for a given set of conditions, including:

- a specific output voltage value
- the total integrated capacitance
- a current profile, specifying the initial and final average current values of the step change

The transition time is taken as instantaneous, which guarantees that the value given by the LCTA is an upper bound value for all logic load operation. If the final current cannot be reached in a single transition safely, then the LCTA can be used to determine the intermediate step to use to achieve the final current safely. Or, the LCTA can indicate how much internal capacitance must be inserted to reach the desired performance.

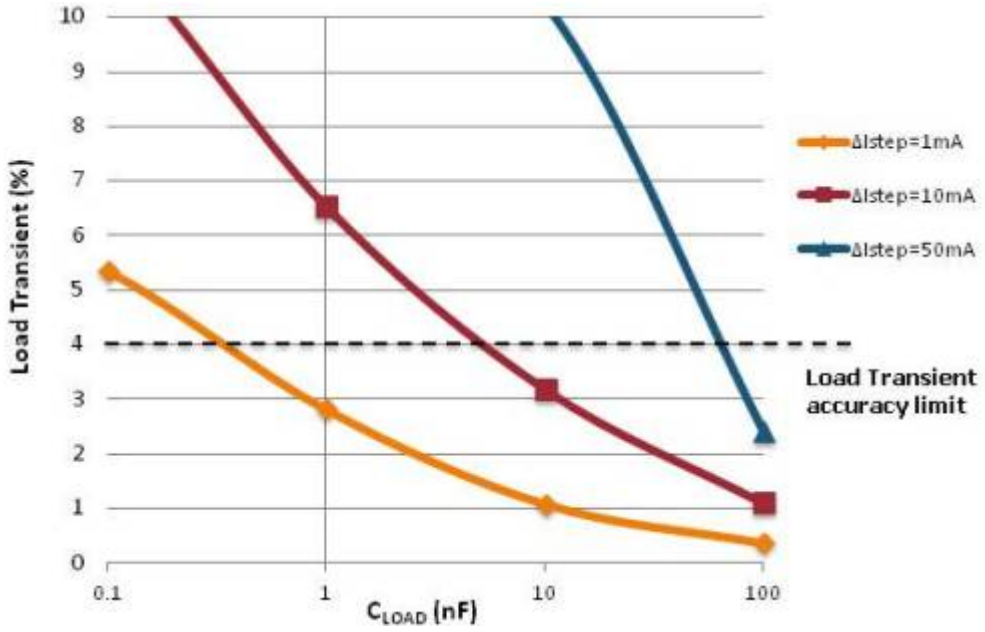


Figure 5: Example of Load Current Tolerance Abacus (LCTA)

6. Simulating Load Transient with PowerVision

PowerVision is an EDA platform including a library of simulation models for addressing a lack in current design flows, particularly in terms of verification of the Power Regulation Networks (PRNet) at the architectural level.

Indeed, the SoC architect can now benefit from advanced verification methodologies for assessing the impact of Noise Propagations and Mode Transitions over the whole System-on-Chip. The Noise Propagation Checks (NPC) enable the validation of the actual impact of power supply noise on performances of analog functions (e.g. High-resolution converters or RF

modules), while the Mode Transition Checks (MTC) enable to verify the impact of voltage variations during power mode transitions.

The adequacy between the load current profile (inducing the load transient response of the voltage regulator) with the expected Load Current Tolerance Template is one of the PowerVision MTC. Indeed, current load variations induce, through the PRNet impedance, voltage fluctuations which shall impact system operation and performances.

Once the on-chip capacitance and load current profile is estimated, application specific voltage variations can be more accurately verified with a MTC in PowerVision, thereby allowing for optimization of multiple transitions when transiting between critical SoC modes. Furthermore, PowerVision enable refinements to be made during the entire design flow if needed.

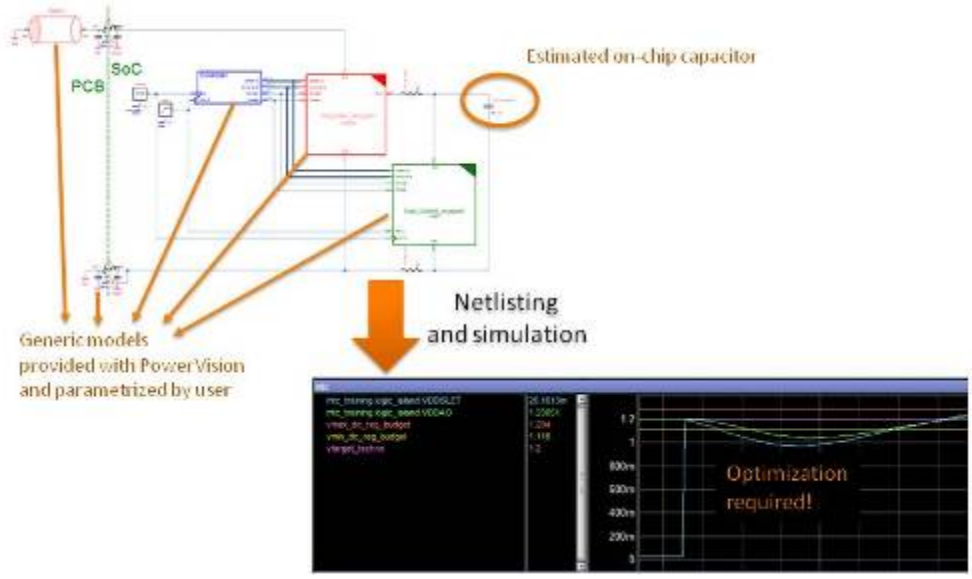


Figure 6: Example of Load Transient validation with PowerVision

7. Conclusion

With an attractive approach for specifying the load transient performance, Dolphin Integration enables a breakthrough to secure the integration of capless voltage regulators. With only a current profile and a load capacitance, the Load Current Tolerance Abacus (LCTA) provides an easy way to ensure internal supply integrity. Thanks to PowerVision EDA platform, Dolphin Integration then enables its users to secure the integration and move forward to further optimizations and verifications.

About the author

Alain Lacourse is Application Engineer for Power Management IP at Dolphin Integration since 2009. He holds a Physics Engineering Master's degree in Semiconductor Devices and Technology, from École Polytechnique de Montréal.

Dolphin Integration IPs

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