Pairing Sensitive RF with Voltage Regulators for Noise-Free IoT Modules

1. Introduction

Internet of Things (IoT) applications are getting numerous, more power-stringent and smaller with every generation, requiring tighter control of power management and maximized function integration. This includes the integration within the same SoC of power-efficient voltage regulators and noise-sensitive modules (e.g. RF) that must be supplied with the appropriate level of noise immunity. This article presents the challenge of pairing an RF analog circuit with the appropriate inductor-based embedded Switching Regulator (namely eSR, equivalent to on-board DC/DC) allowing to meet both the power efficiency requirements and the module performance level at the same time.

2. RF SoC Block Diagram and Low Frequency Noise Sensitivity

Most IoT System-on-Chips (SoC) include core processing, memories (often with data retention capabilities), always-on logic, I/Os, and some analog or mixed-signal functions. Bluetooth (BT) and Bluetooth Low-Energy (BLE) SoCs also embed a baseband module (BB) to process the data to be transmitted or that were received, and an RF system to mix data in and out of the carrier signal.

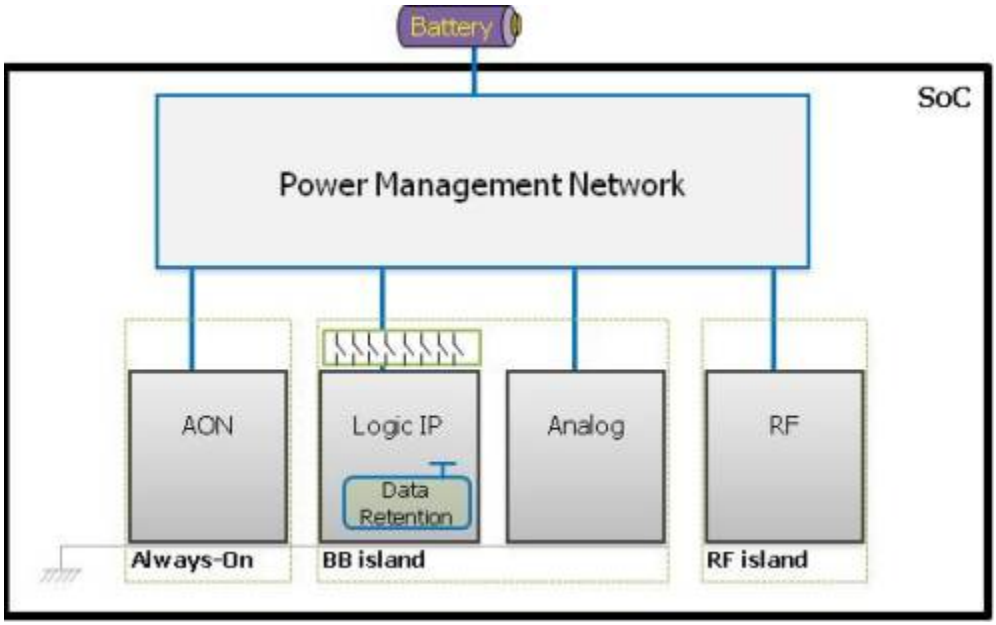

Figure 1 - IoT System-on-Chip

The carrier signal in those standards has a frequency ranging from 2.4 to 2.4835 GHz depending on the selected channel. The baseband module encodes data into a 1 #MHz signal that will be mixed with the carrier signal in the RF module. Therefore, the system will be sensitive to noise in the 1 MHz band, and so, keeping noise low into that frequency band is required. The data converters are generally operating at a higher frequency, so noise at those frequencies will also need to be considered.

Moreover, spectrum emissions in the adjacent band and out-of-band frequencies are subject to specific requirements. Therefore, noise in the range of a few MHz from the carrier will also be of importance in most applications.

3. Noise Sources and Propagation Channels

Many noise sources exist in a SoC and they must all be well identified in order to verify the impact of each propagation path on the noise-sensitive loads, as illustrated in the figure below.

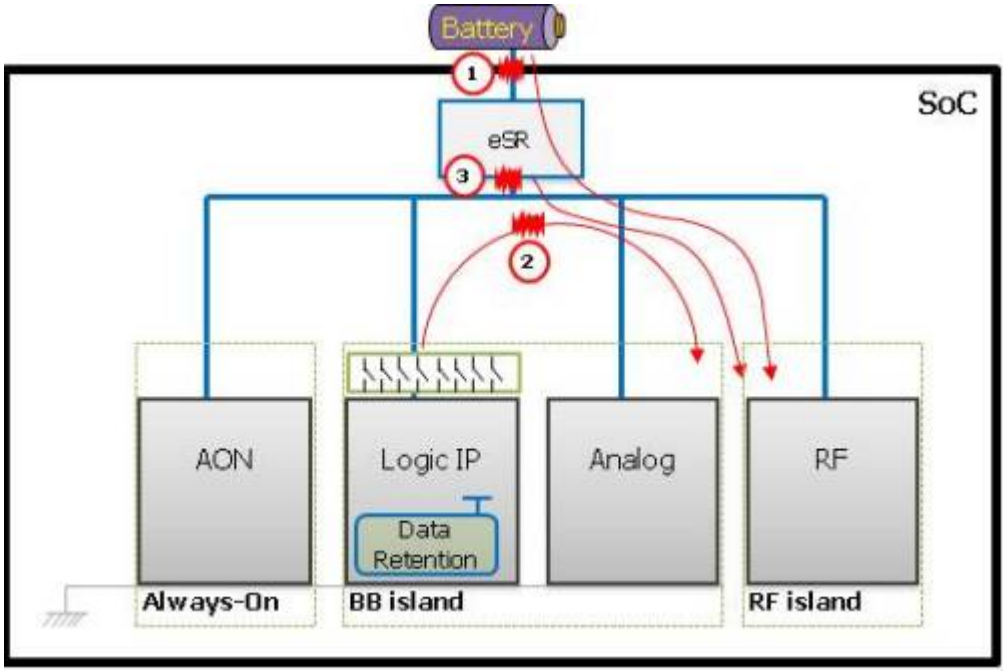

Figure 2 - Noise sources and propagation channels

Batteries (1)

Most IoT applications are supplied using batteries, and they have very low inherent noise, but they also have an internal serial resistance that will produce a voltage variation when the current drawn by the various parts of the system is varying.

Power Supplies (1)

Power supplies and adapters dedicated to charge the battery might be used as an alternative power source for the system while charging the battery. Those supplies often involve switching components and thus can have ripple and noise on their output.

Side Loads (2)

When many loads share the same supply or regulator output, one load might affect the others through the power rail. Current spurs and mode changes of one load will induce voltage variations which depend on the impedance of the regulator output combined with the power distribution network (PDN). The PDN is the network of passive and parasitic components between the regulator and its loads.

Regulator Output Noise (3)

Switching regulators (eSR) are power-efficient: they enable to consume merely as much as power as used by the load. However, voltage ripple is inherent to switching regulators (eSR) and is a maintained voltage oscillation on the regulator output at a fixed or variable frequency. Switching regulators operating in PWM mode (Pulse Width modulation) have a ripple at a fixed frequency, but those operating in PFM mode (Pulse Frequency Modulation) have a ripple at a frequency that depends on the load current (ranging from about 100 kHz down to a few Hz in extremely low-current situations). In the latter, the amplitude of the voltage ripple is also a function of the load current. Ripple is also seen at harmonics of the switching frequency (see figure below). Since the PFM ripple amplitude and frequency may be hard to predict, it might be convenient to force the regulator to operate in PWM mode and then filter the known ripple amplitude in a more limited frequency range, at the cost of a slightly lower power conversion efficiency. Considering only the ripple fundamental frequency without harmonics can induce an unexpected performance decrease of the sensitive functions.

For linear regulators, there is no ripple noise: only flicker noise and thermal electronic noise have to be considered, that are much lower than the ripple of an eSR. These type of regulators thus are good to filter noise from an upstream supply. However, linear regulators are much less power-efficiency than switching regulators.

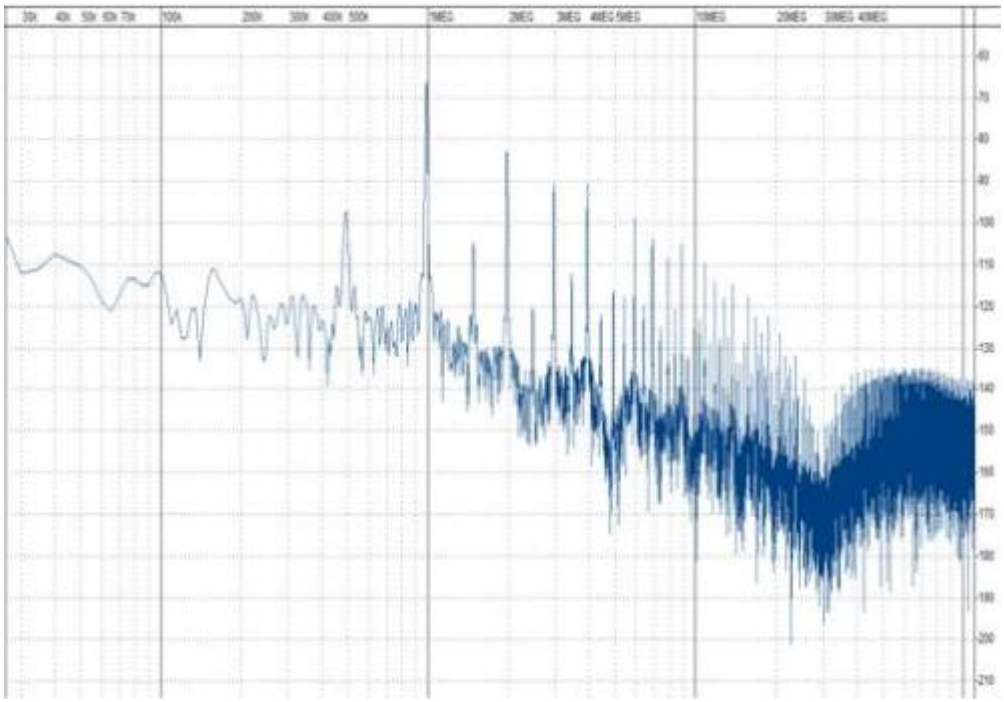

Figure 3 - eSR typical ripple output noise

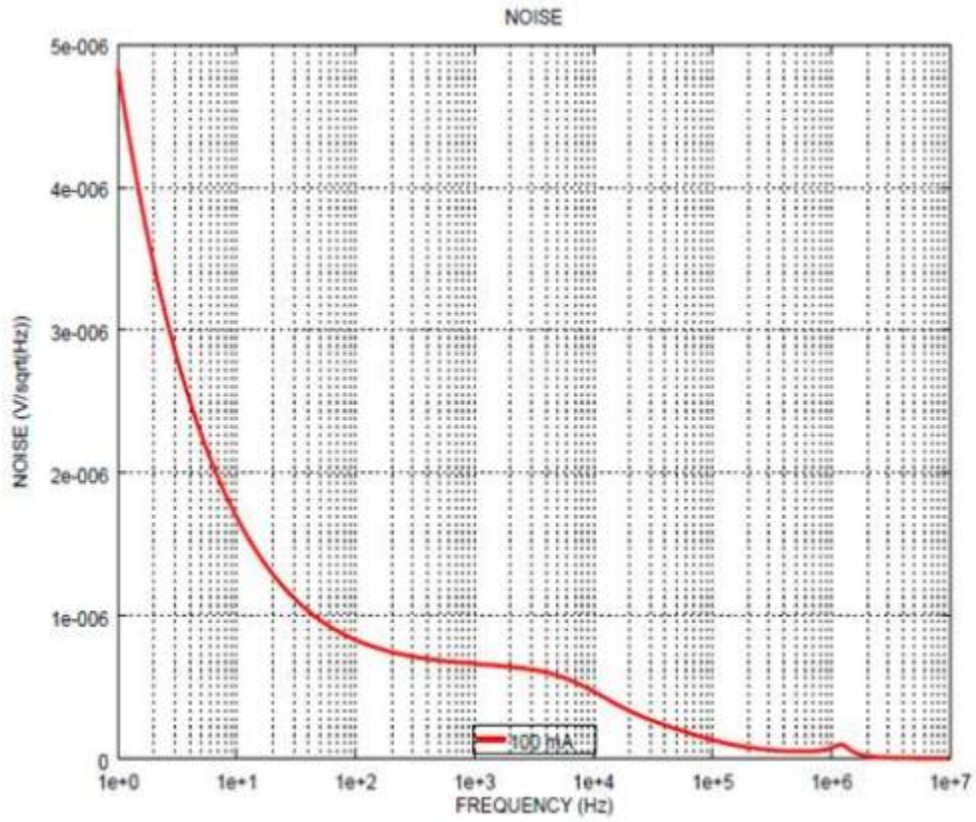

Figure 4 - Linear regulator typical output noise

4. Power Regulation Networks

Several Power Regulation Networks (PRNet) can be envisioned for supplying all loads, depending on the targeted trade-off between power consumption, area and Bill of Material (BoM), which can result in more or less attractive SoC depending on the application.

For example, in PRNet 1 (top of next figure), a switching regulator (eSR) supplies all blocks, both logic and analog. This PRNet offers optimum battery autonomy, reducing the wasted power to a minimum. However, this PRNet might leave the analog (BB and RF) vulnerable to noises caused by the regulator output ripple and by side load activities. Indeed, current changes on side loads (e.g. BB logic) will induce voltage changes through the regulator output impedance and the power distribution network (PDN).

In PRNet 2 (bottom of next figure), a switching regulator converts the power to a closer voltage, and linear regulators (iLR, nLR) regulate down to the final voltage. The nLR is a linear regulator featuring improved power supply noise rejection and reduced output noise than an iLR. This PRNet offers better noise-immunity between loads, but wastes more power

consumption than PRNet 1, occupies more silicon area and will imply the use of more external components (BoM).

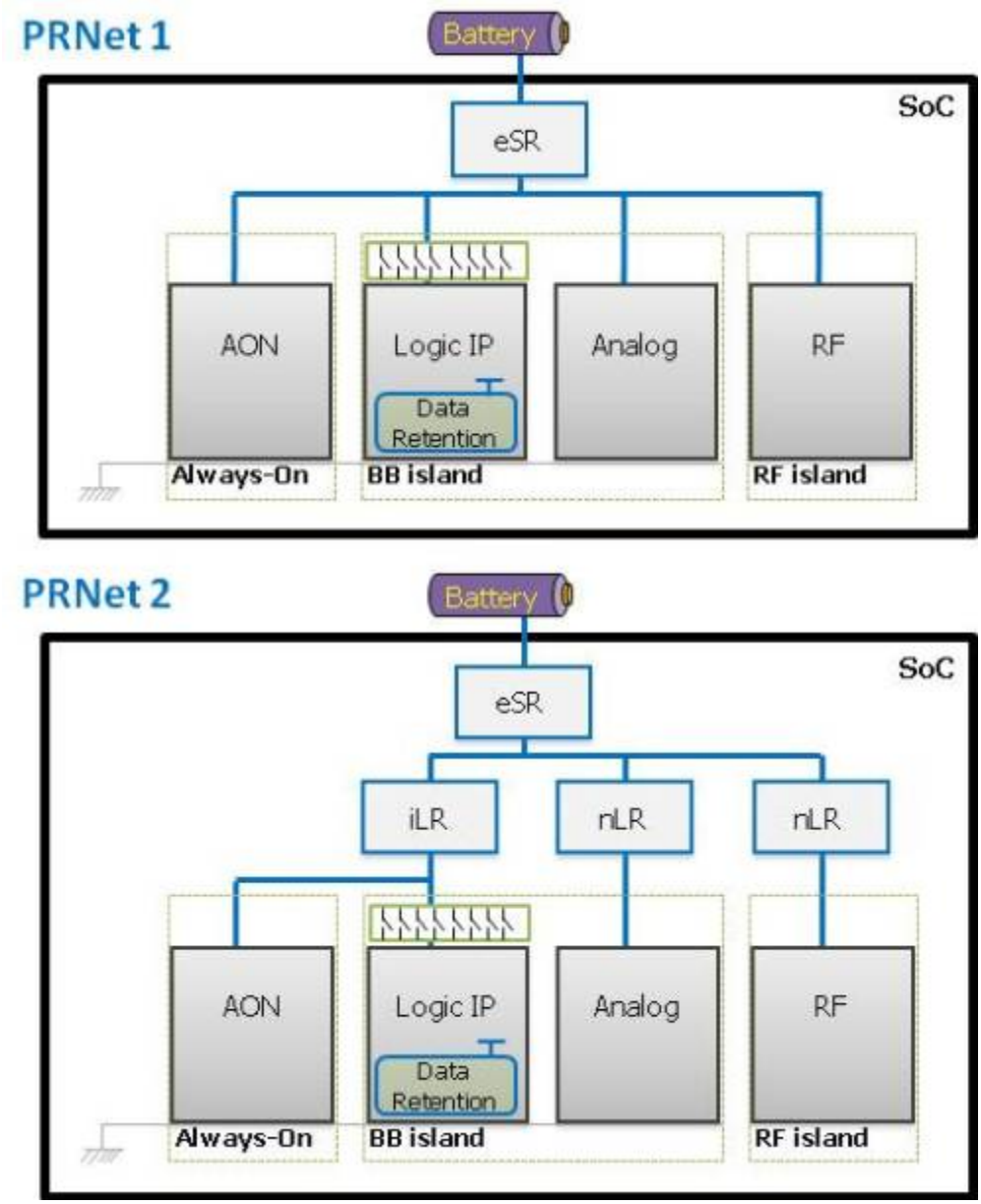

Figure 5 - Possible power regulation networks

5. Quantifying Noise Level Versus Noise Sensitivity of RF loads

To achieve the expected performance of the system, all noise sources must be combined at the supply input of the sensitive block. This results in the maximum noise profile that could occur on the block supply input, and is called the Power Supply Noise Profile (PSNP).

In order to assess the contributions of all noise sources at the supply of interest, the regulator transfer functions PSNTF, CBTF, and Zout are pivotal.

The PSNTF (Power Supply Noise Transfer Function) enables to assess the resulting noise level at the output of a regulator depending on the noise present at its input. This function is often only specified at a single frequency (generally specified as PSRR), thereby giving an inaccurate indication of the actual behavior of the regulator across the entire frequency spectrum. The PSNTF gives the complete information.

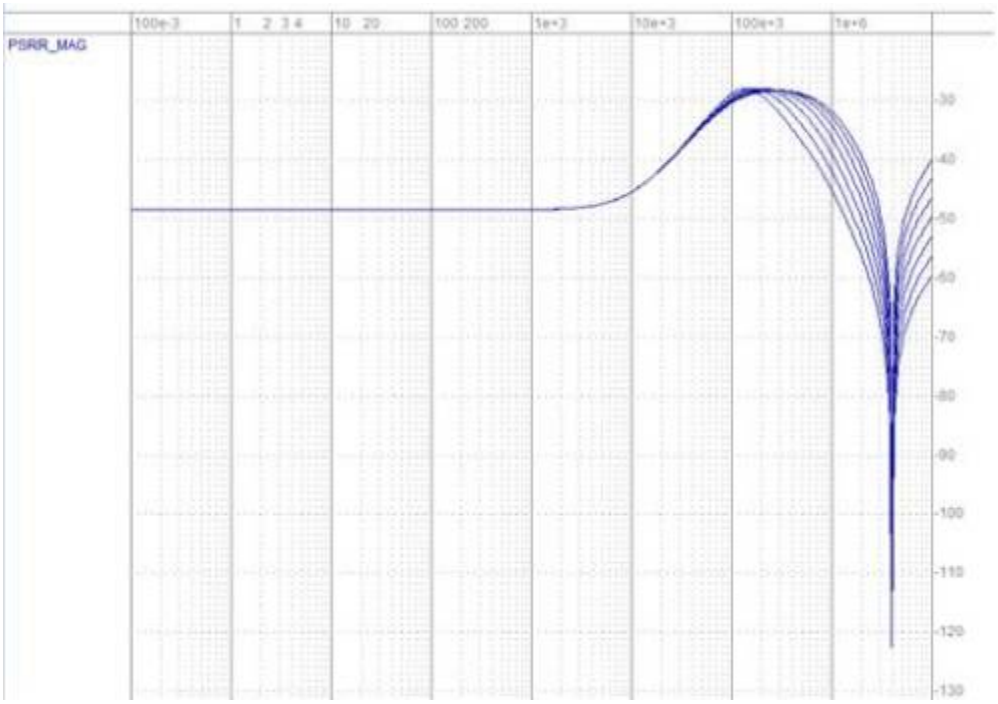

Figure 6 - PSNTF transfer function for various load currents (given in dB vs frequency)

The CBTF (Current Backward Transfer Function) gives the regulator input current drawn from its source for a given current drawn by the load. It is used to evaluate the regulator input current profile induced by the load current profile (LCP).

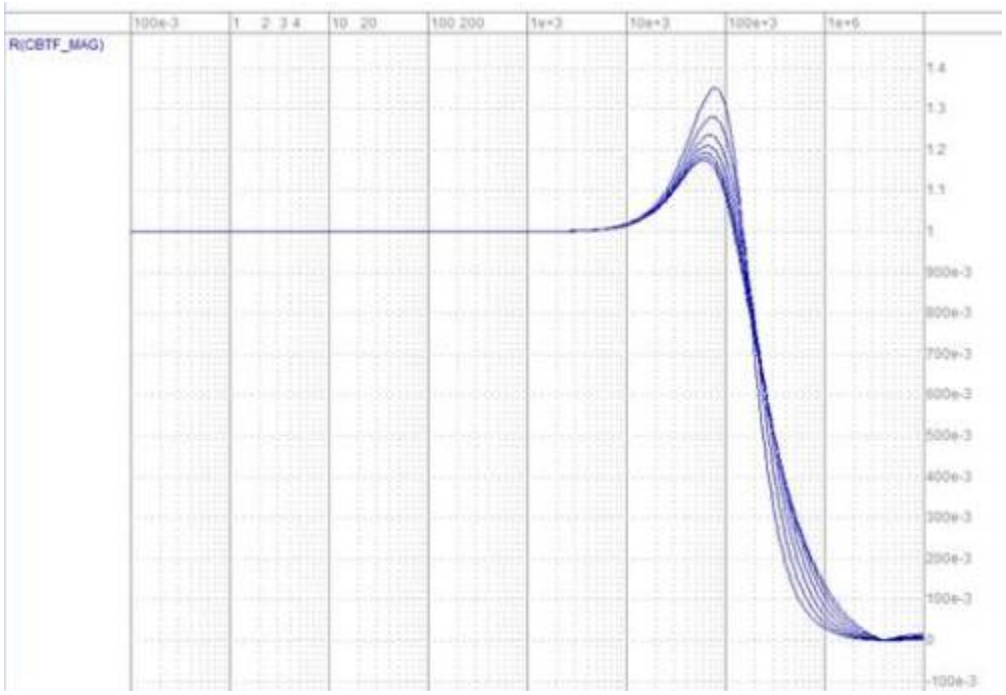

Figure 7 - CBTF transfer function for various load currents (vs frequency)

The output impedance (Zout) is the regulator response to load current changes. The Zout enables to assess the noise induced by the regulator load or to optimize the power distribution network (PDN).

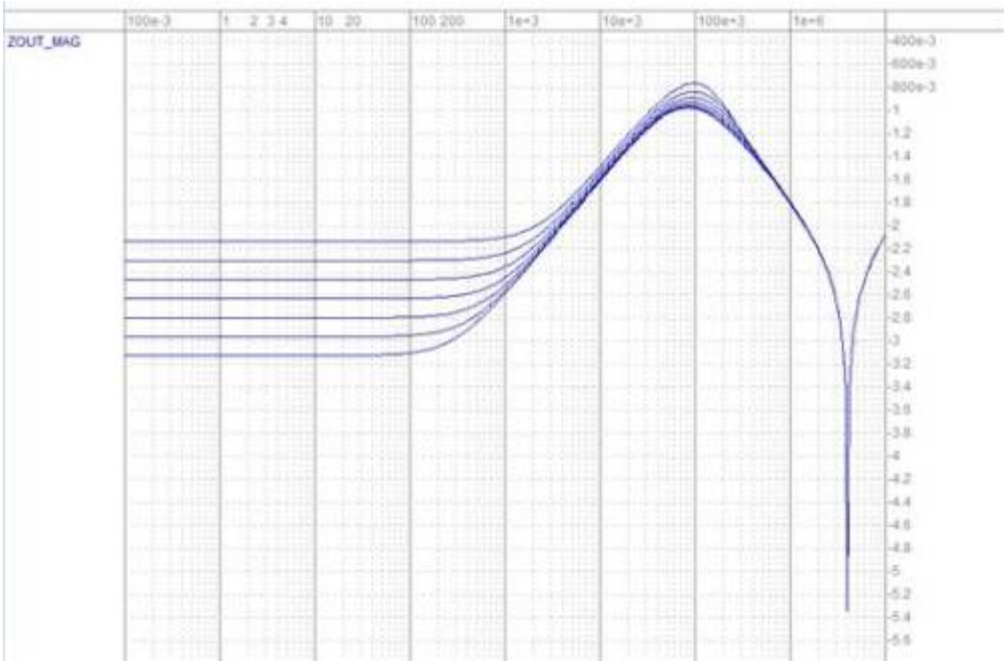

Figure 8 - Zout transfer function for various load currents (given as log(Zout) vs frequency)

Thanks to these transfer functions, the noise sources can thus be evaluated at the supply of sensitive blocks. The resulting Power Supply Noise Profile (PSNP) is then compared against the maximum noise spectrum that can be tolerated on the corresponding supply in order to guarantee the expected performance (for instance, performance of Signal-to-Noise Ratio – SNR – of the sensitive module). This maximum spectrum is called the Power Supply Noise Tolerance Template (PSNT2). The PSNT2 is dependent on the nature and design of the function and can only be extracted by the designer, either by small-signal analysis, in the case of linear functions, or transient analysis, in the case of non-linear or switched functions.

If the PSNP does not meet the PSNT2 then some form of filtering is required, either by using a dedicated regulator, some passive filtering components such as bypass capacitors and ferrite beads, or by revisiting the PRNet and the selection of regulators.

6. PMNet Assessment Examples

Let's consider a RF block that is not too sensitive to noise as a result of robust architecture and design, and that has a PSNT2(A) of 1 mV/sqrt(Hz) over the entire spectrum. The eSR output ripple PSNP(1) of PRNet1 shows a fundamental frequency peak of 0.8 mV/sqrt(Hz). Thereby, the PSNP of the eSR meets the PSNT2 requirement of the RF load and the eSR could be used to supply directly the analog function in this case.

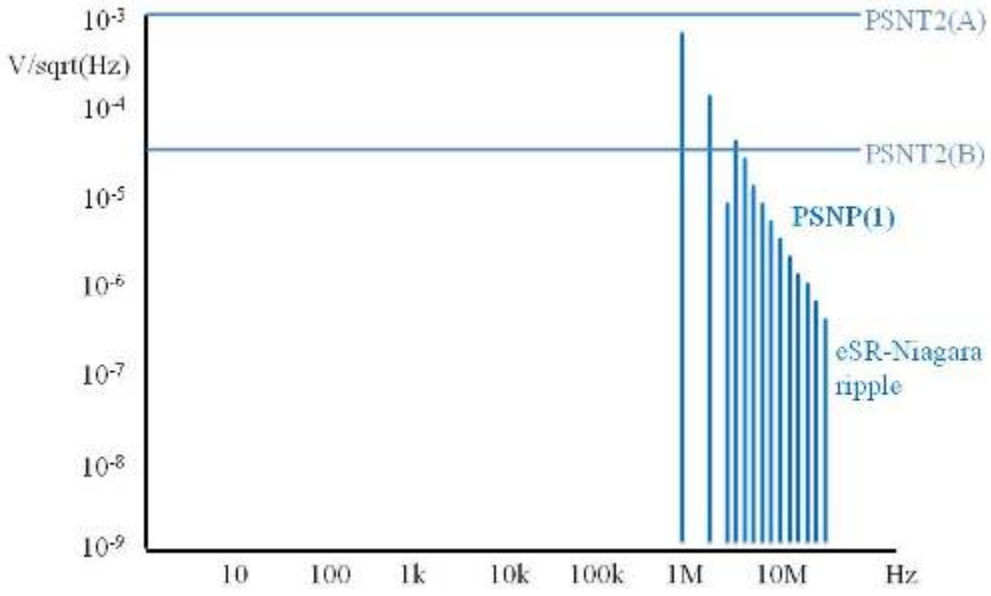

Figure 9 - Comparing PSNP of eSR and PSNT2 of load

Now let's consider a more restrictive PSNT2(B), at 10 µV/sqrt(Hz), resulting from a RF targeting higher SNR performances, thereby being more noise-sensitive. Now the PSNP(1) of PRNet1 exceeds the PSNT2(B) template and some filtering is required if one wants to use an upstream

eSR to lower the main supply, while maintaining power savings. The figure below shows that the nLR (low-noise Linear Regulator), with -40 dB of noise rejection (PSNTF) in the 1 to 6 MHz range, brings the eSR output ripple within the boundary of the PSNT2(B) (see the resulting PSNP in green). It is also noted that the output intrinsic noise spectrum of the nLR also meets the PSNT2(B).

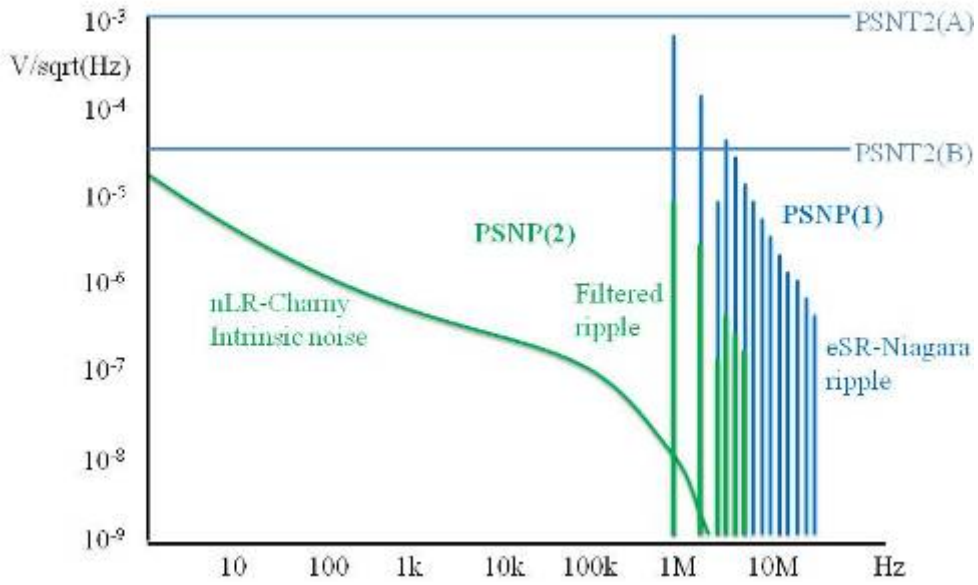

Figure 10 - Comparing PSNP of nLR and PSNT2 of load

A similar analysis must be conducted to verify if a side load current profile (e.g. of a logic block) can affect the performance of the analog function. The load current profile would be multiplied by the equivalent impedance of the regulator output impedance combined with the Power Distribution Network (PDN), and the result would then be compared to the PSNT2.

7. Conclusion

Asserting whether a PRNet is adequate to properly supply a noise-sensitive load such as an RF function requires an appropriate evaluation. This can only be done if the relevant transfer functions and profiles are available across the full spectrum.

Dolphin Integration's advanced regulator specifications include those transfer functions and profiles, thus enabling the integrator to perform the needed noise verifications at the earliest time, thanks to the "profile vs template" methodology.

For moving forward to accurate SoC verification, Dolphin Integration then complements its specifications with advanced models that enable to proceed with simulations of noise propagation channels at the SoC-level.

Related IPs

eSR-Niagara-Bu-dm-ref-[1.62-3.63]-[0.8-2.5].01
https://www.dolphin-integration.com/index.php/silicon_ip/ip_products/description/power_management/eSR-Niagara-Bu-dm-ref-1.62-3.63-0.8-2.5.01_TSMC_55_uLPeF

iLR-Victoria-ref-[1.62-3.63]-[0.8-2.5].02
https://www.dolphin-integration.com/index.php/silicon_ip/ip_products/description/power_management/iLR-Victoria-ref-1.62-3.63-0.8-2.5.02_TSMC_55_uLPeF

nLR-Charny-ref-[1.62-3.63]-[0.8-2.5].03
https://www.dolphin-integration.com/index.php/silicon_ip/ip_products/description/power_management/nLR-Charny-ref-1.62-3.63-0.8-2.5.03_TSMC_55_uLP

About the Author

Alain Lacourse is Application Engineer for Power Management IP at Dolphin Integration since 2009. He holds a Physics Engineering Master's degree in Semiconductor Devices and Technology, from École Polytechnique de Montréal.

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"Foundation IPs" includes innovative libraries of standard cells, register files and memory generators as well as an ultra-low power cache controller. "Fabric IPs" of voltage regulators, Power Island Construction Kit and their control network MAESTRO enable to safely implement low-power SoCs with the smallest silicon area. They also star the "Feature IP": from ultra-low power Voice Activity Detector with high-resolution converters for audio and measurement applications to power-optimized 8 or 16 and 32 bit micro-controllers.

Over 30 years of experience in the integration of silicon IP components, providing services for ASIC/SoC design and fabrication with its own EDA solutions, make DOLPHIN Integration a genuine one-stop shop addressing all customers' needs for specific requests.

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