# Speed up your analog simulations thanks to Dolphin Integration's solution

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## ABSTRACT

SMASH [1] is a seamless IC-PCB mixed-signal simulator enabling the development and verification of analog and mixed-signal Silicon IPs and Integrated Circuits (IC) as well as the optimization of application schematics thanks to its unique multi-domain capabilities. Getting quick transient analysis results of large analog circuits without sacrificing accuracy is a decisive stake. Integration of a new analog solver in SMASH is an important step in this direction. It delivers a 2X to 30X performance increase for simulation run time on a single core.

**Keywords**: analog, simulation, speed-up, performance, solver, SPICE, VERILOG-A, VHDL-AMS.

## 1. INTRODUCTION

Analog designers depend on Spice simulators for accurate circuit analysis; unfortunately, Spice simulations of large circuits are desperately slow. These last years, EDA vendors have introduced fast-Spice simulators which offer a compromise by sacrificing accuracy to speed-up simulations. Unlike our competitors, this is not a suitable solution at Dolphin Integration to guarantee the proper operation of our low power and very high resolution IP converters used in metrology or audio. This is why we choose a new analog solver for SMASH based on KLU, the Sparse Direct Linear Solver from Dr. Timothy Alden Davis [2]. While ensuring the accuracy offered by a global-convergence solver, the main advantages are twofold:

- High speedup for large circuits,
- Increase of capacity in size to simulate large circuits.

These two points will be described in next paragraphs.

## 2. NEW ANALOG SOLVER RESULTS

Simulation run time of different SPICE and VHDL-AMS circuits are published below. In SPICE, circuit size mainly depends on the number of transistors and the number of nets. In VHDL-AMS, the size is linked to the number of quantities.

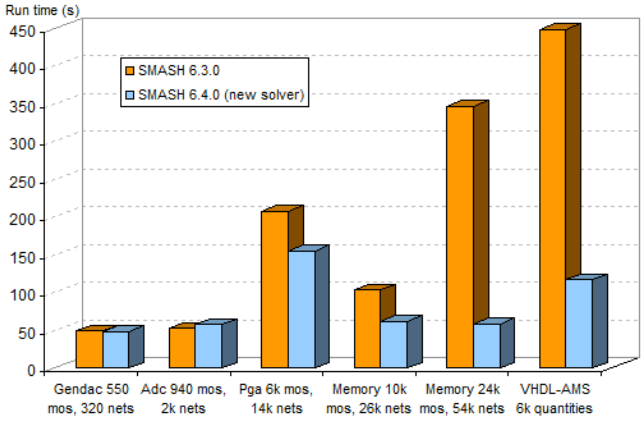


**fig. 1: SMASH simulation run time**

In figure 1, each given run time corresponds to the sum of the important steps of a complete simulation: Loading + Operating-point search + Transient simulation.

We observe that the new analog solver (SMASH 6.4.0) brings obvious benefits on SPICE circuits which have at least some ten of thousands of nets. Indeed, simulation run time of a circuit with 10k mos elements and 25k nets is two times faster than with the previous solver (SMASH 6.3.0). Simulation run time of a large circuit (24k mos elements and 54k nets) is accelerated 7 times.

Moreover, we note a significant 4X gain for a VHDL-AMS circuit with 6k quantities. These five circuits are reflecting the potential of the new analog solver, but there is no specific rule to estimate the gain with the new solver for each circuit. We globally observe obvious gain starting from 10k nets for SPICE simulations and some thousands for VHDL-AMS. This can be explained in next section.

## 3. DETAILED RESULTS

The new analog solver mainly influences one phase in analog simulations of large circuits: operating-point search. This is detailed in the following histogram.

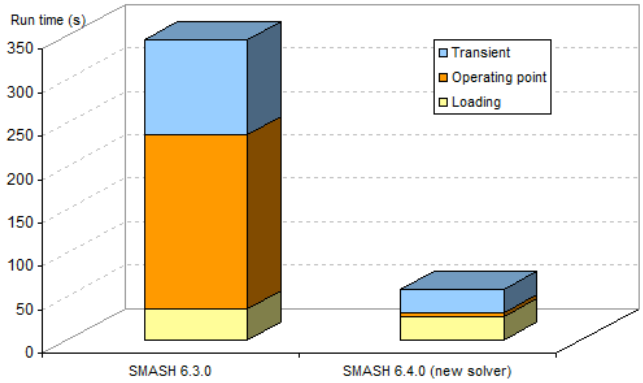


**fig. 2 : Memory 24k Mos - Simulation run time details**

The histogram in figure 2 of a large circuit with 24k mos elements shows that operating-point search phase is accelerated 40 times with the new analog solver, whereas transient simulation is sped-up by a factor 4.

## 4. OPERATING POINT SEARCH STEPS

In order to understand the impacts of the new analog solver on operating-point search, we have measured different steps of this phase, shown in figure 3 for SMASH 6.3.0 and figure 4 for SMASH 6.4.0 with the new solver.

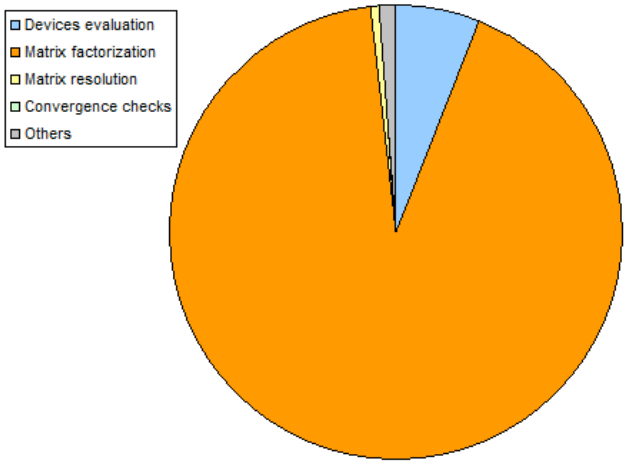


**fig. 3 : SMASH 6.3.0 - Memory 24k Mos - Operating point run time steps**

Figure 3 shows that more than 90 % of the run time during operating-point search is spent in the matrix factorization step. This step is purely depended on the analog solver and the matrix size (number of nets). The larger the matrix is, the longer this factorization step is.

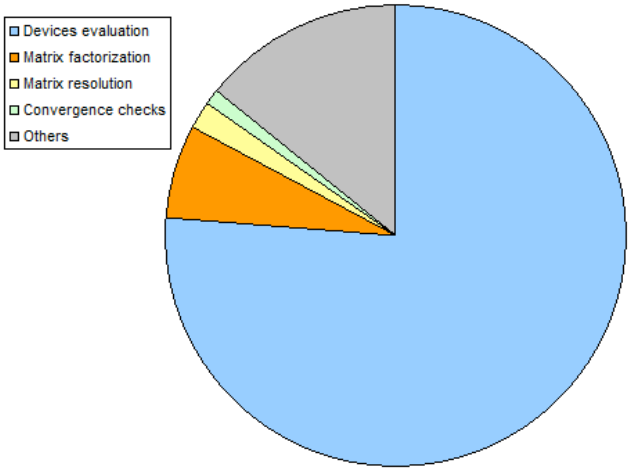


**fig. 4: SMASH 6.4.0 (new solver) - Memory 24k Mos - Operating point run time steps**

Figure 4 shows that, with the new analog solver, the factorization phase has been considerably accelerated and represents only 6 % of operating-point run time. Three quarters of the run time are spent in the evaluation of SPICE devices which is independent from the analog solver.

## 5. IMPACT ON LARGE CIRCUITS

The run time reduction of complete simulation is very crucial for any designer. On large circuits, the new analog solver can reduce simulation run time from some weeks or months to some days, and some hours to some minutes. This can be noted on a large SPICE circuit with 131k mos elements and 425k nets.

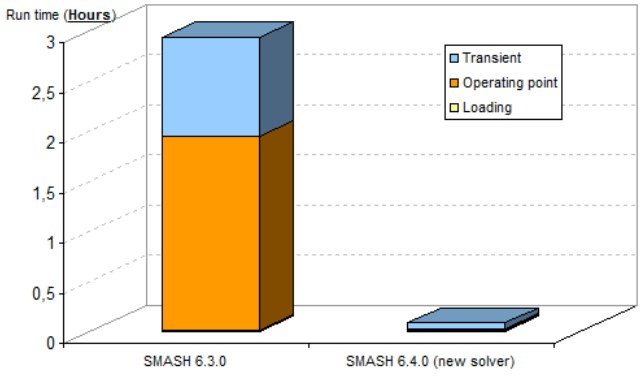


**fig. 5: Memory 131k Mos / 425k nets - Simulation run time details**

The histogram in figure 5 shows that SPICE simulation run time of large circuit is sped-up significantly by a factor of 30. Thus, simulation run-time goes from nearly 3 hours to 5 minutes.

## 6. CONCLUSION

This new analog solver has been successfully integrated into our mixed-signal simulator SMASH. This is a crucial step for analog simulation with SPICE, VERILOG-A and VHDL-AMS in order to simulate accurately large circuits; typically for doing final verifications of complex analog or mixed blocks, such as audio codecs, switching regulators, high sensitivity accelerometers, high performance closed-loop gyroscopes, etc. Moreover, this new solver highlights anew SMASH as a serious and competitive analog and mixed-signal simulator.

This new solver integration is proposed as a technology preview for the June 2015 release of SMASH 6.4.0. It will be available by default for the December 2015 release of SMASH 6.5.0.

## REFERENCES

[1] Mixed-signal simulator SMASH is developed and commercialized by Dolphin Integration, enabler of mixed signal Systems-on-Chip. http://www.dolphin.fr/index.php/eda_solutions/products/smash/overview

[2] Matrix resolution and solver are performed using SuiteSparse, a suite of sparse matrix algorithms. http://faculty.cse.tamu.edu/davis/suitesparse.html