How to make THE difference in power management architecture

To reduce the Bill-of-Material (BoM) and to simplify their usage, System-on-Chips (SoC) become more and more complex due to the integration of a large number of features previously located on board. This increase of complexity, combined with economic and green stakes leads to draw new optimizations, such as partitioning the SoC in different subsets with power and voltage islets supporting several states of activity. Theses states allow minimizing power consumption for islets that are not used or are operating with reduced speed performances.

Embedding the Power Management Network (PMNet) enables a second pass of optimization towards reduction of BoM and power consumption. One of the main challenges for SoC Integrators is then to properly select the PMNet - including power regulators, external and internal capacitors - to sustain the voltage drops caused by SoC activity changes (transition when islets are waken up …), but also to take critical decisions on the integration and the package assembly.

A new generation of power kit library is required, to ease the PMNet deployment and its reuse in successive circuits, to improve the Time-To-Market and to secure the PMNet integration into SoC.

The RPKL approach

Along the lines of RISC architecture (Reduced Instruction Set Computer) is an alternative approach compared to CISC (Complex Instruction Set Computer), RPKL (Reusable Power Kit Library) architecture is driven by a different approach from usual CPKL (Custom Power Kit Library), having all its regulators designed, sized, and assembled for a specific usage.

For those SoC integrators using custom power-regulation kit library to build PMNet, the challenge is that such an offering leads to:
- Either optimize the PMNet architecture with a bottom-up approach for each load in a SoC (modifications of regulators are required to match the needed output current, voltage ranges…) - partaking in a hardly reusable library, an increase of time-to-market, and the risks associated with taping-out a new or modified design.
- Or to create an "all-in-one" regulator that can do it all but is under-optimized for integration on SoC.

To prevent this pitfall, the guiding idea is to define a limited number of power regulators enabling a large spread of usage. To fit this need, an RPKL is based on 30

structural components (or main functions) that can be derived to produce a total of about 350 functional components (or specific functions or combinations).

- Structural components correspond to the main functionality achieved by the component (regulator type, principle of operation, specific performances). They represent a common part which remains constant for all the functional components based on the same structure.
- Functional components are "real" components that deliver up to a pre-defined output current and output voltage range. One of the main characteristics is a resizable pass transistor in linear regulators or switches in switching regulators (aka power stage unit).

The figure below illustrates this principle for a linear regulator. The structure remains the same and the power stage unit is interchangeable. This organization enables to select the appropriate structure for the earlier stages of the SoC architecture, with the flexibility to select the exact functional component in later SoC integration stages.
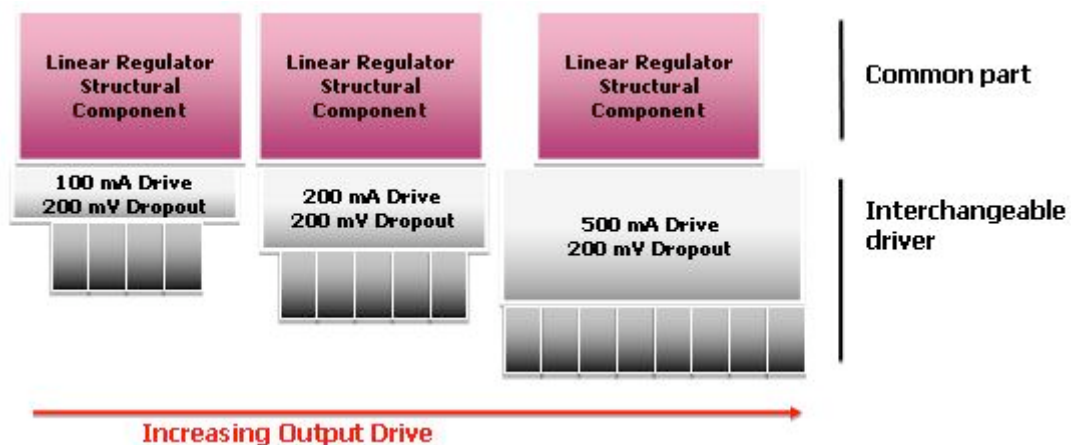

Figure 1: Example of structural and functional components for a Linear regulator

A Reusable Power Kit Library based on only 30 structural components enables to address different challenges among which:

- Low-cost, by providing for example regulators that do not require external tank capacitor to reduce the BoM.
- Low power, by providing regulators that are specifically designed to supply low-voltage and ultra low power mode applications.
- Low noise, for SoCs embedding analog features sensitive to noise on their power supply voltage, such as RF stages, clock oscillator and PLL when a low jitter is required, or high performance analog and mixed-signal functions.
- High efficiency, by providing different variants of power-efficient Switching Regulators (eSR).

The flexibility of the RPKL comes with the use of several pre-defined Interfaces of Distribution of Power (IDP). The IDP represents the connection in a cascade of regulators, or between a regulator and its loads. It enables to split the constraints between upstream and downstream regulators, for example by keeping high voltage constraints only on upstream regulators (area saving). It also enables trade-offs

between higher conversion efficiency, area, BoM and the need for noise immunity in SoCs embedding many islets. The figure below gives a representation of IDPs.
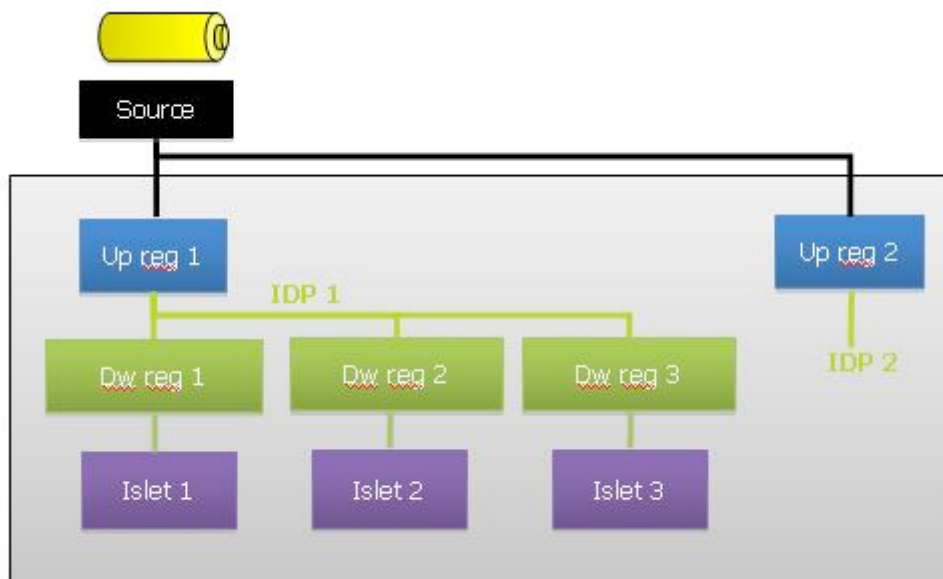

Figure 2: IDP representation

Based on the analysis of tens of block diagrams for diverse applications - such as power metering, smartcard, smartphone, Bluetooth, wireless connectivity, tablet, industrial MCU, smartwatch, RF, or DTV -, from 180 nm to 28 nm, it is possible to affirm that only 4 different IDPs voltages are required for an RPKL.

The IDPs thereby set the standard for regulators input and output voltages; and these voltages are also common in systems so they can also be used to supply I/Os and peripherals.

Nevertheless, building a PMNet implies to verify it, and also to perform the verification from the earlier stages of the PMNet definition and optimization, up to the completion of the physical implementation. To address this need, specific views (simulation models) are provided to verify the adequacy of the PMNet with its loads in different operations scenarios to make sure that:
- The power supply voltage of each IDP will remain in the operating range of each load during the transition from one operating mode to another (MTC: Mode Transition Check).
- The noise generated on the power supplies by the different loads across the PMNet will not degrade the performances of noise-sensitive loads (NPC: Noise Propagation Check).
- The integration is properly structured and sized (assembly, routing, decoupling, etc.)

These views must be provided as a standard deliverable for each functional component of an RPKL, together with some guidelines for facilitating their usage.

Benchmarking methods

There are multiple alternative solutions to build the PMNet for a given SoC. The obvious one is to optimize component-by-component, for example by getting the best efficiency for some regulators without taking into account the impact at the global network level or of induced BoM and area cost. Other parameters such as the load activity over time and the other regulators involved in the PMNet have to be considered,

A more reliable solution to identify the most suitable PMNet is to define different constructions of the PMNet and to compare them using a common Figure of Merit (FoM). A FoM is an arbitrary function that weights various parameters together in order to optimize a set of performances (power, cost, battery life, etc) and deduce the best compromise. It follows that a FoM is application-specific and its form will be selected based on those performances factors.

As a starting point, the FoM can be chosen to get the best area and power consumption trade-off by minimizing both the SoC power consumption and the SoC or PMNet area.
It leads to find the minimum figure for the formula FoM = area x power (mm^2 x mW).

As an illustration, the following example represents the different loads for a SoC. The SoC is powered thanks to a battery and spends most of the time in wait mode. The optimization at application level can be either cost (BoM, SoC area) or lifetime operation (Low power).
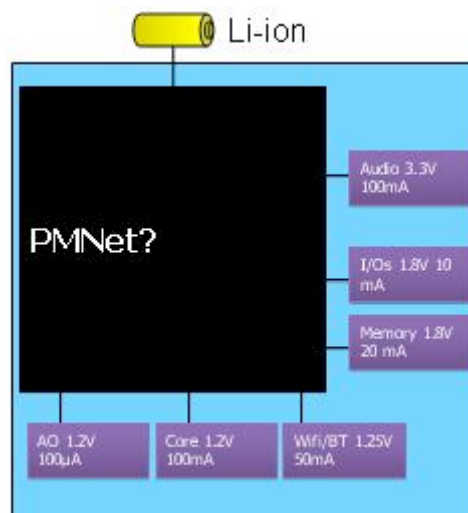

Figure 3: Loads to be supplied by the PMNet

4 different synoptics have been drawn with different approaches:
-   1- Power optimization (higher efficiency for each regulator)
-   2- BoM optimization (reduction of the number of external devices)
-   3- Optimization of the power consumption during SoC activity
-   4- Optimization of the power consumption during SoC wait mode

In the synoptics, the following regulator types are used:

- eSR: **e**fficient inductor-based **S**witching **R**egulator
- iLR: **i**slet **L**inear **R**egulator
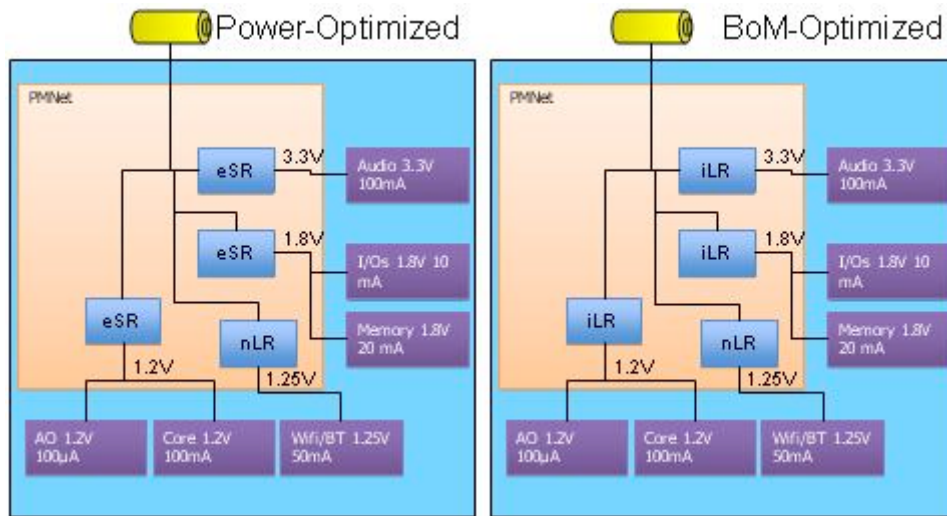- nLR: low-**N**oise **L**inear **R**egulator
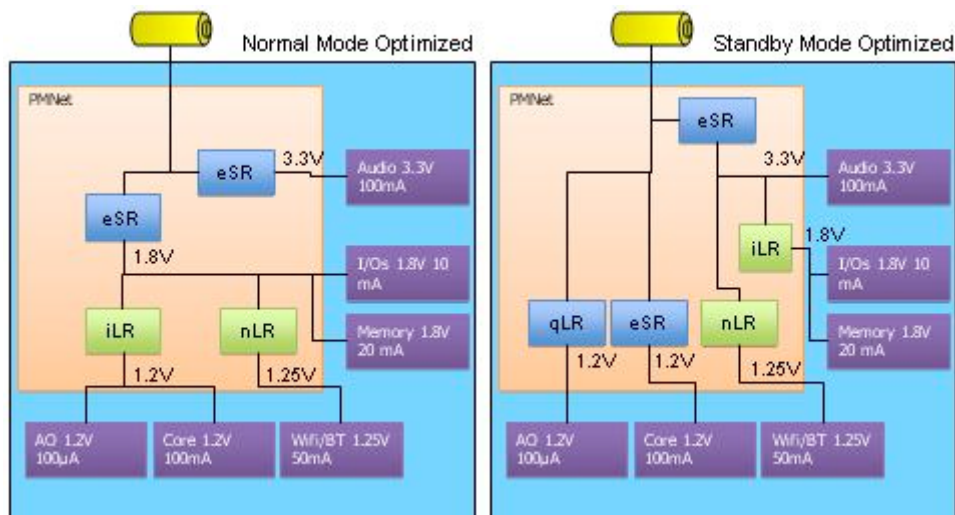

Figure 4: PMNet synoptics 1 and 2

Figure 5: PMNet synoptics 3 and 4

The figure-of-merit below represents independently the power and area "performances" for the different synoptics. Synoptics 1 and 3 have similar power performances, whereas synoptic 2 has the lowest area but the highest power consumption. To enable to select among these 3 synoptics, the used FoM enables to weight each criterion.

Figure 6: FoM for 4 different PMNet synoptics

In a situation where both area and power consumption of the PMNet must be optimized, synoptic 2 turns to be the optimal solution.

Conclusions

The RPKL arrangement into structural and functional components allows a high flexibility and opens the door to its reuse into other SoCs. The RPKL enables fast time-to-market and right-on-first-pass integration into SoCs. Since there are many possible optimizations of PMNet for a given SoC, selecting the appropriate one can be eased by using the appropriate FoM that can be enriched to match with the targeted application.

Before launching a complete library of products based on the RPKL principle, proof of concept has to be checked thanks to Silicon Qualifiers in different process nodes. Associated verifications have also to be demonstrated in order to enable to anticipate by simulation the behavior and performances of the PMNet and its associated loads.

Indeed, it is not only necessary to prove that power-regulators individually meet their specifications, but also that all interactions are properly mastered, simulated and measured: IR-drop, Pop-Up Noise, transitions between modes of power domains, high-frequency disturbances on high-resolution converters.

About the author
Sebastien Genevey
Dolphin Integration

Sebastien Genevey received the Master's Degree in Integrated Circuit design from the Polytechnic Institute of Montpellier, France. He enters to Dolphin in 1997 as analog designer for mixed-signal products. He is currently CTO for analog developments for audio, metrology and power management products.

About Dolphin Integration
Dolphin Integration contribute to "enabling mixed signal Systems-on-Chip". Their focus is to supply worldwide customers with fault-free, high-yield and reliable kits of CMOS Virtual Components of Silicon IP, based on innovative libraries of standard cells, flexible registers and low-power memories. They provide high-resolution converters for audio and measurement, regulators for efficient power supply networks, application optimized micro-controllers.

They put emphasis on resilience to noise and drastic reductions of power-consumption at system level, thanks to their own EDA solutions missing on the market for Application Hardware Modeling as well as early Power and Noise assessment. Such diverse experience in ASIC/SoC design and fabrication, plus privileged foundry portal even for small or medium volumes, makes them a genuine one-stop shop covering all customers' needs for specific requests. http://www.dolphin-integration.com