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Multiplexed Energy Metering AFEs Ease ASIC Integration and Provide Significant Cost Reduction

Christian Domingues, Analog Designer, Dolphin Integration

Smart electric meters are fundamental to the successful deployment of smart grid technology, as they improve grid reliability and user consumption control and reduce electricity theft. The variety of consumers' emerging needs requires a much wider offering of energy metering systems-on-chip (SOCs), paving the way for more fabless companies to enter the energy measurement field. Energy meter-specific analog front-end (AFE) devices, which combine high performance with cost reduction, are thus needed to complement standard IC offerings.

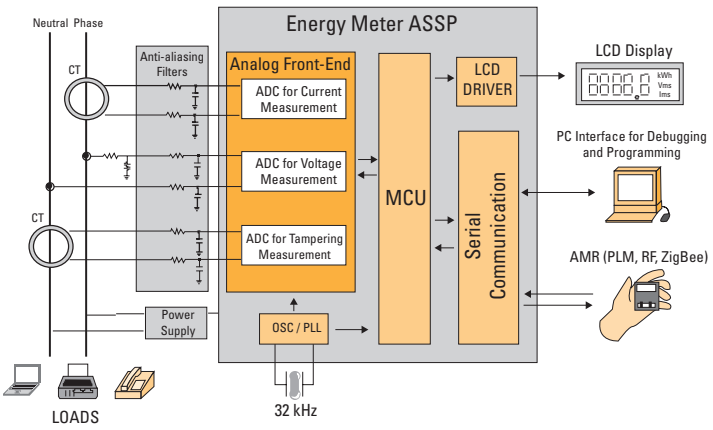
Today's energy metering standards demand higher accuracy and lower power consumption which, in turn, challenges system designers to deliver more competitive AFEs. This article reviews those challenges and presents a solution based on a multiplexed channel architecture that delivers ultra-high resolution, along with very low-power consumption and silicon area. First, the article gives an introduction to smart electric meters and their specifications. Second, it presents the architecture used in conventional energy meter AFEs, and compares the trade-offs of using a high-performance analog-to-digital converter (ADC) versus using a lower performance ADC together with a programmable gain amplifier (PGA). Third, a new multiplexed AFE architecture for three-phase energy meters, which yields considerable area and power savings while simplifying the integration of application-specific ICs (ASICs), is detailed. Finally, the need for multi-domain simulation to guarantee AFE performances at the system level is discussed.

Smart Electric Meters

Electric meters, also called Ferrari's e-meters, are simple metal disks rotating in a magnetic field due to induced currents. They were first introduced in residential houses at the beginning of the 20th century and were used until the last decade when the electricity industry started to adopt electronic meters. Smart electric meters are beginning to replace the old meters because they offer higher accuracy and require less power at a considerably lower cost. Furthermore, they offer additional functional benefits such as real-time reading, tampering detection, remote reading and service power outage notification.

Figure 1 shows the architecture of an application-specific standard product (ASSP) for single-phase energy meters with tampering detection, which is used by many manufacturers. The ASSP contains an AFE to convert the analog input signal given by current and voltage sensors into digital information. Digital signal processing is used to compute the different energy metrics such as instantaneous, active and reactive power; voltage/current value; and power factor. A microcontroller unit (MCU) manages the system and its peripherals (e.g., real-time clock, liquid crystal display (LCD), communication ports/modules). Current transformers (CTs), resistive shunts and Rogowski coils can be interfaced to the AFE to measure current, while resistive bridge and voltage transformers are used to measure voltage.

Figure 1. System Block Diagram for a Single-phase Energy Meter



Standard Compliance

Energy meters are specified according to their class and range, which are defined by European International Electrotechnical Commission (IEC) and American National Standards Institute (ANSI) standards. Its class refers to the accuracy of measure, and its range refers to the dynamic range across which accuracy should be achieved. Each standard also specifies environmental requirements, such as how much power the meter itself can dissipate and how much voltage it must tolerate. Classes between 0.1–2 meters with ranges between 500–3,000 and greater are available today.

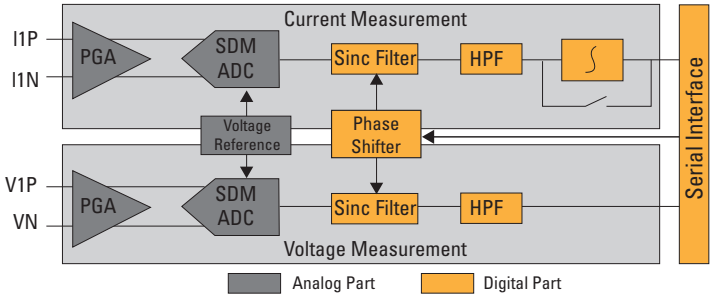
From the Energy Meter Class/Range Specification to the AFE Performance Specification

The AFE is critical in meeting application objectives since it provides the link between the real world and the processing world. To ensure standard compliance, the SOC integrator must be able to translate the class/range specification to the AFE fundamental requirements commonly known as signal-to-noise ratio (SNR), input referred noise voltage or equivalent number of bits (ENOB). An energy meter with a class of 0.1 and a range of 1/1,000 must measure active power with less than 0.1 percent error over a current variation of 1,000 to 1 or better. For such a class/range target, the ADC should resolve a minimum detectable signal of 1 µVrms over a dynamic range of 1 Vrms, which requires it to have a SNR of 120 dB or an ENOB of 19.6b. It is also important to understand that the AFE error budget is much less than 0.1 percent in relation to the total error meter budget. Assuming a CT with 0.07 percent accuracy requires an AFE accuracy of 0.07 percent with a 123 dB SNR ADC.

Conventional AFE Architecture Used in Energy Metering

As previously discussed, an energy meter with a class of 0.1 and a range of 1/1,000 requires an AFE with a resolution of 19.6b. One approach used to achieve this class/range specification uses a high-performance ADC with accuracy better than 19.6b. Such virtual component (ViC) ADCs are available, but are not cost-competitive for energy meter applications. Figure 2 presents a more cost-competitive solution for single-phase meters which allows the same class/range specification to be achieved. This architecture uses a PGA including automatic gain control (AGC) to increase the AFE input voltage to the required ADC dynamic range, and a ΣΔ ADC with lower performance (16b ENOB) in the current path. The voltage path is composed of the same 16b ENOB ΣΔ ADC and a PGA with smaller gain values (1–2), as the voltage line variation is usually less than ±10 percent. The digital part allows for phase shifting compensation between the current and voltage path and offset removal, and Rogowski coils can interface thanks to digital integration.

Figure 2. Conventional AFE Used in Electricity Meters



Compared to a high-performance ADC architecture, a PGA and ADC architecture provides many more advantages, including:

- Easier implementation.
- Reduced area and power consumption.
- Evolution to a higher range specification since ViC ADCs with accuracy higher than 21b are not available.

Solutions Expected from a ViC Provider that Broaden the Marketplace for Power Metering SOCs

Nowadays, ViC providers must provide support to SOC integrators developing energy meter SOCs that can compete with standard ICs. The ViC provider should offer:

- A cost-effective solution that occupies a small silicon area and requires few external components.
- A high-resolution and low-power solution because of regulatory standards and customer requests for increased dynamic range and accuracy.
- A understanding of the application constraints and proper specification of the ViC.
- A modular library containing several ADCs, PGAs and voltage references to answer the various needs of power metering solutions and reduce time-to-market.

Solutions that can be used to meet these expectations are discussed in the following sections.

Reducing the Cost of High-Performance Energy Metering ICs: Multiplexed ADC ΣΔ Application to a Three-phase Energy Meter

Today, the major challenge facing SOC integrators is reducing the cost of energy meter SOCs while maintaining high accuracy. Figure 3 presents two distinct methods used to achieve a three-phase energy meter with a class of 0.1 and a range of 1/1,000:

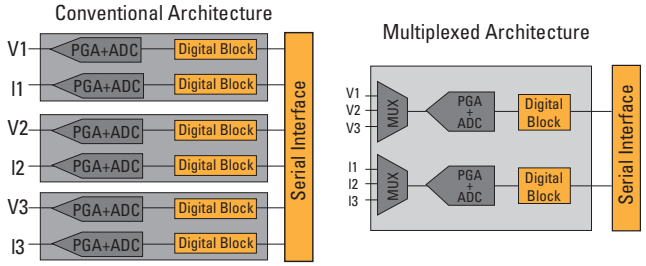
- A standard solution, where currents and voltages are sampled simultaneously via parallel ΣΔ ADCs.
- A multiplexed architecture, where currents and voltages are sampled using faster ΣΔ ADCs.

For the past few years, multiplexed successive approximation ADCs have been used in low-end energy meter applications that don't require high accuracy. When targeting high-end applications that require high accuracy and wide ranges, the ΣΔ modulator becomes incontrovertible. The multiplexed AFE presented in Figure 3 uses a three-input analog multiplexer, a low-noise PGA with gain steps between 1–32 and a 16b ΣΔ modulator with a sampling rate of up to 4 kSps. It requires an analog multiplexer frequency of 12 kHz for a measurement bandwidth of 2 kHz. Since the current in each phase can be different, the embedded AGC evaluates the input signal amplitude and controls the preamplifier gain at each multiplexer cycle.

Until recently, ΣΔ ADCs have not been considered appropriate for use in high-end applications with multiple multiplexed inputs because they rely on "sinc" digital filters which have very slow settling responses. To achieve ΣΔ ADC multiplexing, specific low-latency finite impulse response (FIR) filters are used to overcome the drawbacks of sinc filters and to allow ΣΔ ADCs to fully settle on every conversion at rates up to 4 kSps. The proposed multiplexed solution halves power consumption and silicon area compared to the standard three-phase AFE, all the while keeping the accuracy advantages offered by ΣΔ ADCs.

See **Energy Metering** *page 44*

Figure 3. Standard and Multiplexed AFE Architecture for a Three-phase Energy Meter



Architectures using a single ADC with a six-input multiplexer for three-phase energy meters are also available. They allow for sequential conversion of the currents and voltages of the three phases (e.g., phase 1 current, phase 1 voltage, phase 2 current). Nevertheless, the presented architecture which uses two ADCs offers the following advantages in comparison:

- Range specification can be higher since each ADC has only three multiplexed inputs.
- Voltage path requirements are less constraining than current path requirements, which allows a lower accuracy ADC to be used for voltage measurements.
- No extra phase shifting is introduced since voltage and current are converted simultaneously.
- Easier implementation of the digital part.

Advanced Modeling Techniques for Guaranteeing SOC-level Performances

Even if the AFE achieves the required performance, the SOC performance at the system level cannot be guaranteed since AFE performances can be degraded by poor peripheral components and integration within the rest of the SOC. To guarantee SOC performance and yield, the AFE must be validated with the peripheral components required by the ADC (e.g., clock, reference voltage). To perform this simulation in a short amount of time, the following are required: an appropriate electronic design automation (EDA) solution allowing for multi-domain and multi-level simulation; libraries of high-level description models of electronics (e.g., PGA, ADC and digital-to-analog converter (DAC)); and peripherals (e.g., clock, references, power management and sensors). In energy meter applications, there are four sources of inaccuracies in peripheral components that must be taken into account to avoid performance degradation:

- Clock jitter: A jittered clock has two or three subsequent periods which are not equal over time. In ΣΔ modulators, the input signal is sampled at the clock frequency, introducing noise in the sampled signal and, consequently, reducing ADC SNR.
- Reference voltage noise: The reference voltage gives a clean voltage to the ADC. Its noise level should be specified to avoid an increase of the ADC noise floor.
- Reference voltage temperature drift: ADC gain is sensitive to the voltage reference level which in itself is sensitive to temperature. Since a power meter should give the same billing in the winter and summer periods, the voltage reference temperature drift must be accounted for to minimize the ADC gain variation (about 10–50 ppm/°C in class 0.1).
- Anti-aliasing filter mismatch: The anti-aliasing filters shown in Figure 1 are required in front of any ADC to avoid the aliasing of high-frequency components present in the power lines. The mismatch value of the RC external components gives a mismatch on the low-pass filter cut-off frequency, and thus a phase error between the voltage and current path. For example, 10 percent-accurate external components can cause a phase error of about 0.5°, and thus an error in the power measurement of about 1.5 percent.

Using this approach provides the means to check that peripheral component specifications are suitable to meet the specific SOC requirements and highlight possible poor integration.

Conclusion

Integrating high-performance AFEs in energy meter SOCs is now practicable, but it requires close cooperation between the SOC integrator and ViC provider to guarantee standard compliance and appropriate yield. A multiplexed architecture integrating a new filter approach overcomes the performance limitations of conventional ΣΔ modulators, making the AFE for SOC three-phase energy meters more cost-competitive in terms of area and power consumption. ■

About the Author

Christian Domingues began his semiconductor career at the Techniques of Informatics and Microelectronics for Integrated Systems Architecture (TIMA) laboratory, where he worked as an analog research engineer for two years. In 2006, he joined Dolphin Integration as an analog engineer, working in the field of high-performance measurement ΣΔ ADCs. Domingues received a master's degree in microelectronics and a Ph.D. in analog ICs and microelectromechanical systems (MEMS) from the Polytechnical National Institute of Grenoble (INPG) in France in 2001 and 2005, respectively. You can reach Christian Domingues at jazz@dolphin-integration.com.