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Power Management Network Design Methodology and Verification to Secure RFID Product Tape-Out

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Abstract

This paper introduces a parallel association of regulators named Retention Alternating Regulator (RAR) as an innovative solution to achieve the best performances in both normal and retention modes in the context of an RFID active tag System-on-Chip. Very low-power sleep mode applications where the system must run up to many years on the battery have strict power requirements in each mode. Verifications are required to ensure proper operation at all times, especially during the system startup and at mode changes where voltage must be maintained to prevent data integrity. To address this challenge, the Regulator Control Unit (RCU) is proposed as a reliable design technique to ensure a safe transition between two or more embedded regulators.

Biographies

Alain Lacourse has been granded a M.Sc.A. in Physics Engineering from École Polytechnique de Montréal, and cumulates 15 years of experience in the fields of semiconductors and nanotechnology.

Marcel Lapointe has been granted a Ph.D in Electrical Engineering from Laval University, in Quebec, Canada, has been a post-Doctorate fellow at École Polytechnique de Montréal, and has more than 20 years of experience in the fields of telecommunications and power management.

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1 RFID Application Case

A major challenge of the microelectronics industry today remains power management. In RFID-technology-based circuits, reducing leakage current becomes so crucial that combining complex power management features is now required. Integration of regulators in Systems-on-Chips (SoC) does provide many advantages such as reduction of cost, bill-of-Material, and printed circuit board real-estate, and tighter control of power modes.

However, it does also come with its share of issues such as thermal dissipation. The selection of the right regulator early in the design cycle, having optimum characteristics and size, is crucial in product development. It happens often that the exact amount of current consumed by the SoC is known only at the end of the project. Changing the regulator specifications at this stage may result in increase of the initial footprint dedicated to the regulator, and significant floorplan changes. Early assessment using rigorous methodology must then be followed.

RFID systems are based on wireless, non-contact radio frequency energy for communication between a tag and a reader. The tag circuit contains stored data whereas the reader transmits an encoded radio signal to interrogate the tag. RFID systems can thus be classified by the type of tag and reader, which can be either active or passive:

1. Passive tags rely on RF energy transferred from the reader to power the tag. The tag can be used and powered only if passed near a reader.
2. Active tags use an internal battery to continuously power the circuitry whatever the distance from the reader. The battery is often a lithium primary cell that is not rechargeable and must last many years. This puts high constraints on the overall power dissipation.

Such a stringent application implies very low standby current, and somewhat optimized active-mode power. Loads are in the order of mA. Leakage becomes a major criterion that drives the design. The choice of a low-leakage process such as TSMC 180nm uLL becomes important.

This paper presents a specific type of regulator design specifically to power applications where both the normal and sleep modes must be optimized, such as active RFID tags. The product main constituents are presented and then critical verifications to ensure the proper operation are presented.

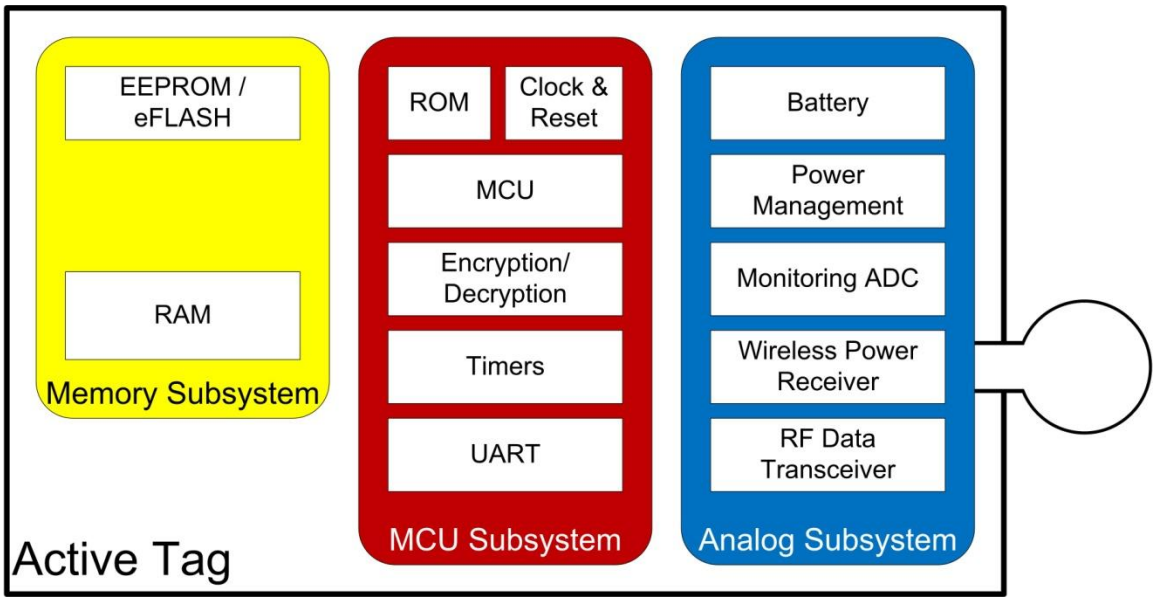


Figure 1 – Tag Functions

2 The SoC Power Modes

In RFID applications the tag is mostly in sleep (or standby) mode, waiting for the reader to initiate the communication. In sleep mode the tag is dissipating low power by retaining the data and monitoring for a reader that would try to initiate the communication. In normal mode, the tag is processing commands requested by the reader and communicating the information back to the reader.

The active (or normal) mode is when most of the SoC activity is occurring : all main functions are active and the dissipation is high, in the mA range. On the other hand, the standby mode is when most of the SoC activity is shut down : only critical functions said "always-on" (AO) are active. The dissipation is then very low, in µA range. Many ways exist to reduce the power dissipation of a SoC. These techniques can impact the dissipation in any mode, either active or sleep.

The logic functions of the SoC related to this paper are realized using transistors in TSMC 180nm eLL process. The normal mode is therefore supplied at 1.8V, the core voltage of this process. The logic gates and memory blocks used have been designed to keep their data and operate down to 1.2V. The regulator output voltage is changed to 1.2V to reduce the leakage in sleep mode.

3 Principle of Operation of the Retention Alternating Regulator

In active mode, the RFID circuit exchanges data with remote circuits via electromagnetic signals. This function needs a large amount of power dissipated by the RFID circuit. The

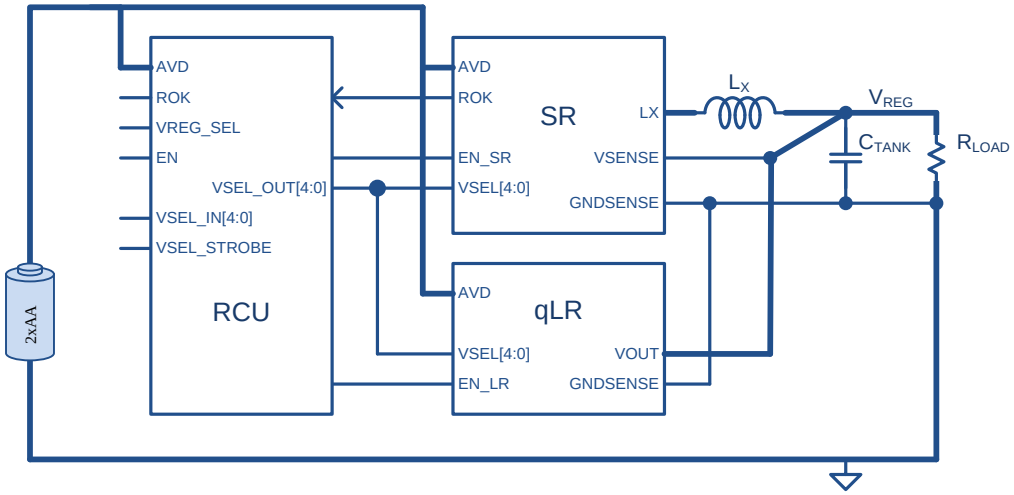
Retention Alternating Regulator (RAR) provides up to 50 mA to supply the RFID circuit and logic in. It is important in this case to transfer the power from the battery to the RFID circuit in an efficient manner in order to optimize the battery life. The RAR block diagram is depicted in figure 2. It embeds two regulation units and a control block. Their operations are described in the following sections. A generalization of this type of regulator is given in the last section.

3.1 Normal Mode

The best way to optimize the power dissipation in the SoC active mode is by implementing a switching regulator (SR) in the RAR, which is an integrated inductor-based switching regulator. When the RAR Normal mode is selected, this regulator is converting power efficiently over a large range of load currents, and it also maintains its efficiency regardless of the battery voltage, provided the battery voltage is higher than the RFID supply voltage plus a minimum dropout of 200 mV. The voltage range allowed at the battery terminals is 3.6 V down to 2.0 V (1.8 V supply plus 200 mV dropout), which is suited for many batteries, including double alkaline batteries (2xAA) and lithium coin cells that do not exceed 3.6 V when fully charged.

The SR operates by modulating the pulses that switch the on-board inductance (Lx) to charge the tank capacitor (Ctank) to the selected voltage. Two types of modulation are realized, depending on the amount of output current drawn by the load. A Pulse-Width Modulation (PWM) is realized when the output current is high, between 5 mA and 50 mA. The efficiency then achieved is between 90% and 95% (assuming an ideal inductance with no equivalent series resistance). The efficiency tends to quickly get worst when the output current gets lower than 5 mA. To remedy this issue a Pulse-Frequency Modulation (PFM) is automatically activated when the output current is lower than 5 mA. The PFM keeps the efficiency higher than 70% down to 0.3 mA (figure 3).

Figure 2 – RAR Block Diagram



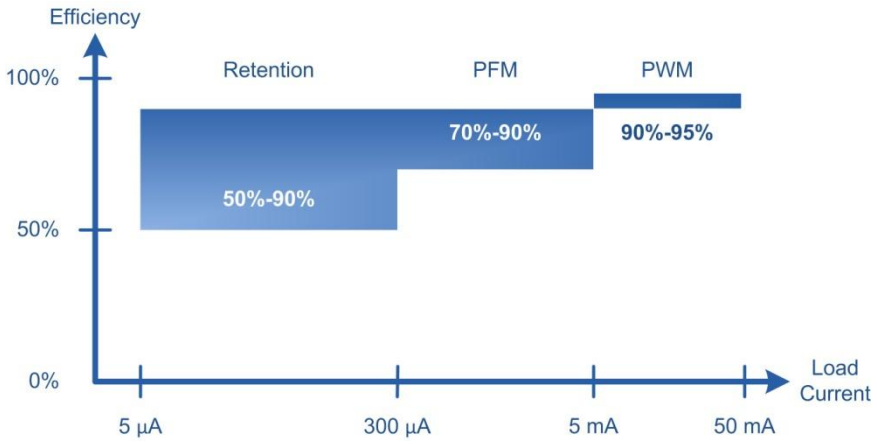


Figure 3 – Efficiency ranges per mode

3.2 Retention Mode

With an output current lower than 0.3 mA it is difficult to maintain the efficiency better than 70% because the SR needs a minimum quiescent current to operate, which is 80 µA for this product. When the output current gets lower than 300 µA, the SR is shut down and replaced by a qLR (low-quiescent Linear Regulator), which is a second regulator implemented in the RAR. The quiescent current of this regulator is as low as 220 nA, which represents 0.3% of the SR's quiescent current. With such a quiescent, the efficiency can be held in between 50% and 90%, provided the battery voltage is in between 2.0 V-3.3 V and the output voltage is at 1.8V.

The RFID circuit of the tag is a digital circuit realized with core transistors that operate at 1.8 V nominal. At this voltage level the logic blocks can run at full speed in normal operation. In sleep mode however the activity is reduced to a minimum by means of two techniques. First, the clock is slowed down in order to reduce the power dissipation due to logic switching. Second, the supply voltage is lowered down to 1.2 V in order to reduce the current consumption of the logic. In sleep mode the RFID current drops below 300 µA, which allows the RAR to turn off the SR and turned on the qLR. This regulation mode is called "Retention Mode" (as opposed to "Normal Mode" when the SR is enabled and the qLR is set to high-impedance (HiZ) mode).

This mode is said "Retention" because it is important to hold the states of the RFID circuit (and the data in the memory circuits, if there are any). This is achieved by generating a minimum voltage to the RFID supply in order to let it alive. On the other hand, the supply voltage must be high enough to allow a minimum activity in the RFID in order to process the eventual incoming data that will wake up the RFID for the next ID service.

Even if the clock activity is reduced to rare events in retention mode, the qLR must provide sufficient current to fulfill the needs of leakage current flowing in the RFID. However, this characteristic is interesting as long as the qLR quiescent is significantly smaller than the leakage to fulfill. For this reason, the qLR quiescent has been specified at 220 nA. This comprises the current consumption of a voltage reference, plus the

circuitry to program the regulation voltage from 1.2 V to 1.4 V by step of 50 mV, and from 1.4 V to 3.3 V by step of 100 mV. In other words, the qLR is a complete regulator with only 220 nA to carry out the retention function.

It is recalled that the outputs of both regulators are put in parallel. While the qLR is enabled when in retention mode, the SR output is set to HiZ to prevent any output conflict. Furthermore, the SR is shut down to reduce the quiescent current. In addition to 220 nA due to qLR, the total quiescent is increased to 270 nA due to the leakage of the SR when set to shut-down mode. Note that 270 nA is still significantly low in comparison with a RFID tag leakage.

One could generalize that the conversion efficiency of a regulator is important when the load current is much higher than the regulator quiescent current. However, when the load current is of the same order of magnitude or lower than the quiescent current, then the regulator quiescent specification is much more important to save power.

3.3 Shutdown Mode

In certain applications or for prototyping reasons it might be interesting to replace the RAR by an off-chip regulator that supplies the on-chip RFID circuit. For these purposes a "Shutdown Mode" is realized in the RAR where both regulators, SR and qLR, are in shutdown mode. In this case, the shutdown current is 50 nA. The RAR quiescent can be considered practically negligible.

In shutdown mode the outputs of both regulators are set in HiZ in order to prevent any voltage conflict with the alternative source.

3.4 Mode Change Time

There is a tank capacitor at the regulated output to supply fast charges to the load . A few microfarads are needed to realize this function. It averages out the bursts of high-amplitude current peaks generated by the RFID when the gates and the flip-flops are switching. In other words, it averages out the load current up to an amount of 50 mA in a bandwidth treatable by the SR.

When the RAR is requested to change from retention to normal mode, there is a time interval when no current is provided by the regulators, because the qLR is faster to be set in HiZ than the SR is ready to provide a large output current. In order to allow the load to quickly resume activity, an interval of 2 µs is specified for the RAR to complete the transition from the qLR to the SR following the VREG_SEL input signal command. Once the SR has completed its startup and is regulating properly, a Regulation OK (ROK) signal is output to confirm that full logic activity can be restarted.

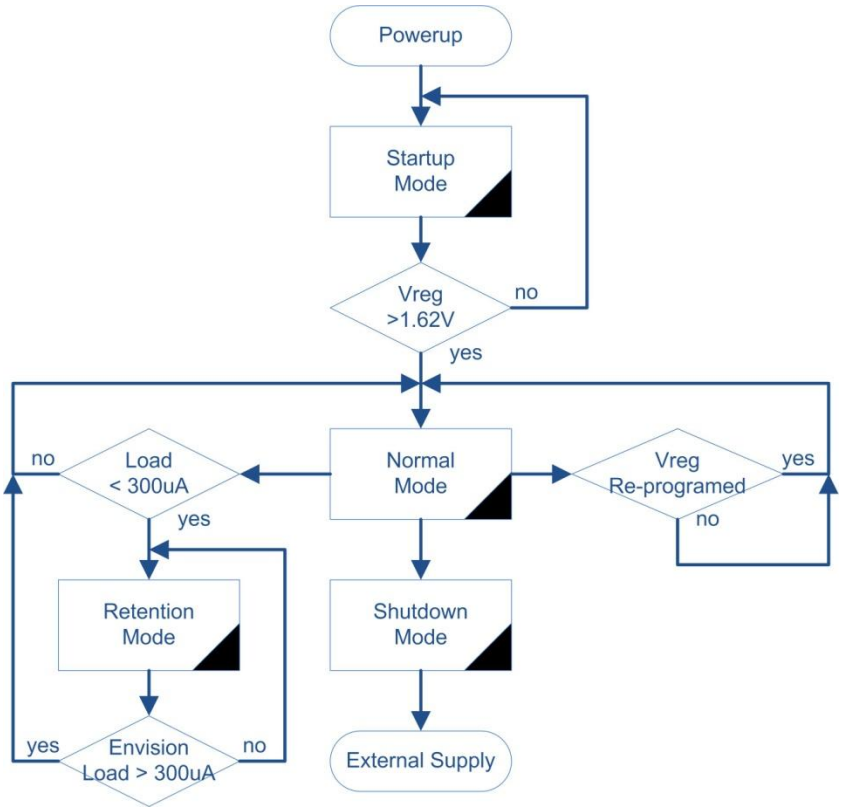


Figure 4 – Regulation Modes

3.5 Regulator Control Unit

Each regulator has its own controls to program the regulated output voltage, to set the output in HiZ, or to set the regulator in shutdown. Because they operate in parallel on the same regulation point, it is important to avoid any conflicts. For this purpose, a third circuit in the RAR, the Regulator Control Unit (RCU), controls the operation of every regulator to program the output voltage and to set them in the different modes. The timing diagram below (Figure 5) illustrates the RAR modes and their transitions. Additionally, the RCU prevents any logic signals to be interpreted until the startup sequence has completed.

3.5.1 Normal Mode

The RCU is controlled by the ACU of the SoC to set the RAR in different modes according to the level of activity the RFID undergoes. For example when an incoming data is received, the treatment by the RFID is fast and complex, which creates a load of tens of mA that the RAR must supply.

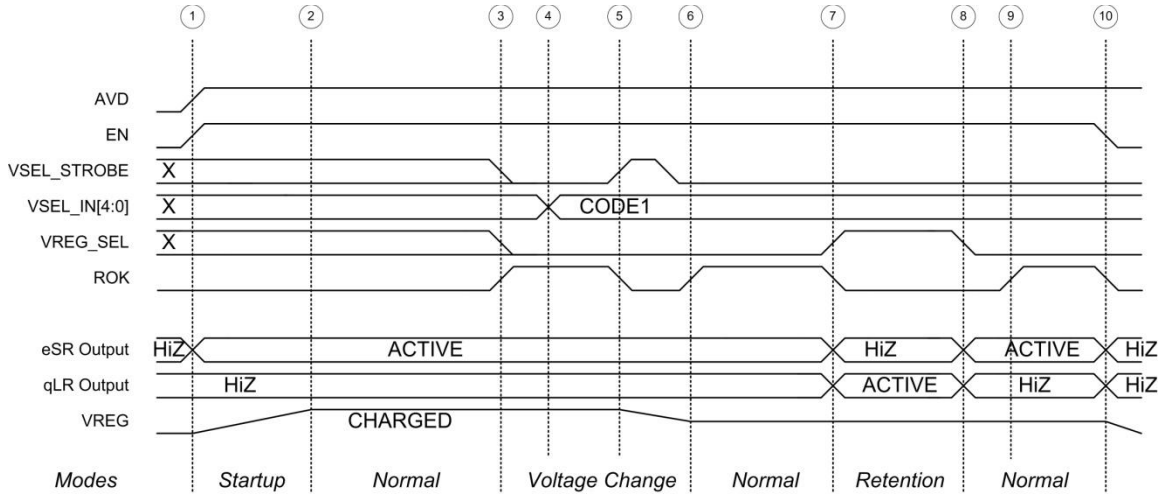


Figure 5 – Timing Diagram

This is done by setting the RCU input VREG_SEL to "0" (Figure 2). In doing this, the RCU sets the qLR output to HiZ, enables the SR and allows the SR output to regulate (not HiZ). All these controls are coordinated by the RCU, which is initiated by the RFID with only one input, VREG_SEL.

In normal mode, the output voltage of the RAR can be re-programmed by the ACU. This is the case, for example, when the ACU prepares to enter the sleep mode in order to save power. Not only the ACU gets ready to slow down the clock, but the supply is lowered to 1.2 V to reduce the leakage. The ACU programs the output voltage by setting a 5-bit bus, VSEL_IN[4:0], which is strobed by the pin VSEL_STROBE. The value is then saved in a register internal to the RCU.

Note that the output voltage can be re-programmed only when the RAR is in normal mode. The reason is that the tank capacitor needs a large current to set a different voltage at its terminals in a reasonable time interval. The only regulator able to generate it is the SR.

Table 1 – Output Voltage Maptable

VSEL_IN[4:0]	VOUT	VSEL_IN[4:0]	VOUT	VSEL_IN[4:0]	VOUT
01000	1.20	10000 (default)	1.80	11000	2.60
01001	1.25	10001	1.90	11001	2.70
01010	1.30	10010	2.00	11010	2.80
01011	1.35	10011	2.10	11011	2.90
01100	1.40	10100	2.20	11100	3.00
01101	1.50	10101	2.30	11101	3.10
01110	1.60	10110	2.40	11110	3.20
01111	1.70	10111	2.50	11111	3.30

3.5.2 Retention Mode

The retention mode is selected by setting to “1” the RCU input VREG_SEL. In doing this, the RCU sets the SR output in HiZ, shuts down the SR, and allows the qLR output to regulate (not HiZ). Again, all these controls are coordinated by the RCU, which is initiated by the ACU with only one input, VREG_SEL.

As previously mentioned, the output voltage can not be re-programmed when in retention mode. Even if new values are programmed at VSEL_IN[4:0] and strobed with VSEL_STROBE, the RCU blocks the selection. The former value is held in a register to maintain the selected output voltage.

3.5.3 Shutdown Mode

The RAR is shut down by resetting the EN pin. Both regulators are then shut down, and their outputs are both set to HiZ. Note that EN takes precedence over VREG_SEL.

3.5.4 Start-Up Mode

The RAR has a special mode when the system is powered up. On the one hand the SoC and its ACU are supplied by the RAR, on the other hand the RAR is controlled by the ACU. To initiate this loop, the RCU takes control of the RAR during the powerup.

During the Startup Mode, all the inputs are disabled, except the EN input. The output voltage is automatically programmed to 1.8 V. The qLR is disabled, whereas the SR is enabled. The tank capacitor is charged up to 90% of 1.8 V by the SR. Once this threshold is reached, the control is given to the ACU. This is done by asserting the ROK output flag. Only at this moment can the ACU change the regulator mode and program another output voltage.

3.6 RAR Principle Generalization

The regulator described above is a specific case of RAR. Generally, a Retention Alternating Regulator embeds two or more regulators controlled by a Regulator Control Unit. The assembly of regulators is designed to optimize many SoC power modes. In the previous sections the SoC active mode is supplied by the SR and the sleep mode by the low-quiescent LR. Replacing the SR by a linear regulator sized to supply 50mA could have been possible to produce a RAR that optimizes the BoM rather than the active mode power. More complex assemblies can be realized but all should have an embedded RCU to manage the power modes and transitions.

4 Integration and Verification

Verifications related to the RAR design, like startup and regulator switching, are already performed by the RAR designers. The inclusion of the RCU has already taken care of most issues related with the operation of the RAR. But, similarly with any embedded

power management network, there are some verifications that need to be performed by the integrator to ensure the proper operation of the RAR within the SoC.

4.1 Maximum Average Current

The first step is to select the appropriate RAR current configuration, the maximum average current the RAR can supply in normal or sleep mode. The load current variations contain high-frequency components that are beyond the regulator bandwidth. Internal and external decouplings are used to filter those currents. This topic is beyond the scope of this paper. The average of this current is what the RAR can supply. The RAR described in this document can supply 50 mA in normal mode and 300 µA in sleep mode. Other configurations are available.

The maximum average current of a logic function is generally not precisely known early in the design. Estimations must be made with margins for errors, and they can be based on past designs and metrics, thereby allowing selection of the regulator maximum current drive or to verify if the selected RAR is fit for this application.

As the RTL and synthesis are completed, a much better assessment of the dissipated power can be made, and some software tools are suited for this task. Past this point, changes would require major layout changes.

4.2 Startup and Sequencing

Startup of the RAR is handled by the RCU until the internal SoC signals from the Activity Control Unit (ACU) are valid. This interaction between the RCU and the ACU must be checked to ensure the SoC will actually get alive after startup.

Also, the transition from normal to sleep mode implies reprogramming the regulator output voltage before switching to retention, and vice-versa. The RAR is delivered with a FTDM view (Functional and Timing Diagram Model). It is a model of the behavior of the inputs and outputs of the regulator, including timings. A logic simulation using this model is therefore required as soon as the ACU RTL has been created.

4.3 Voltage Drop

As described earlier, the RAR can only regulate the voltage for current variation components that are within its bandwidth. Higher frequency variations must be handled by other means: metal routing resistance, bonding resistance and inductance reduction, double-bonding, internal and external additional decoupling capacitance, etc. Care must be taken to ensure the final components and parasitic are within the regulator specifications to ensure performance and stability of the regulator.

A behavioral model can be used to make this verification in the context of the application. Combined with a model of the load and its interconnections, an analog simulation will reveal if the internal voltage drops below critical levels.

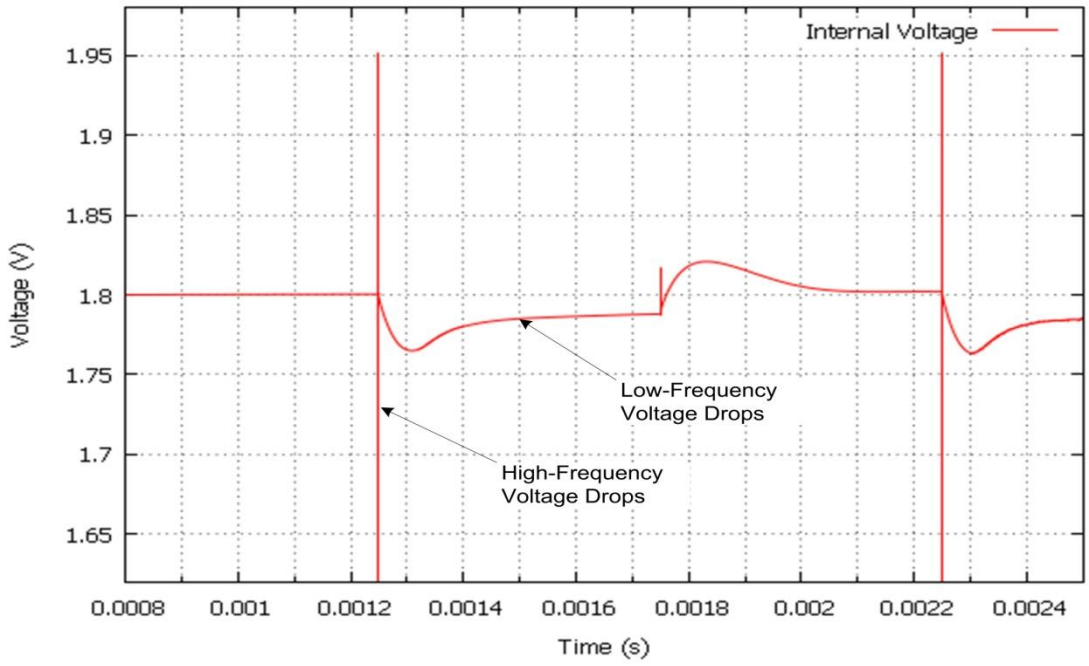


Figure 6 – Activity on a regulation node

5 Conclusion

This paper presents the Retention Alternating Regulator (RAR) used to supply applications in which the power consumption in sleep mode is critical, while the normal mode is still important to optimize, like RFID active tags. The RAR combines a switching regulator (SR) and an ultra-low quiescent linear regulator (qLR) to supply the same load in each mode. A Regulator Control Unit manages the startup while control signals from the Activity Control Unit are not yet valid, and during modes changes to ensure the voltage output integrity. The integrator must perform some verification early and during the integration process to ensure the maximum average current will not exceed the RAR specifications in each mode and to validate transition changes for ensuring a reliable System-on-Chip.