Offer efficient power management and power distribution to your SoC
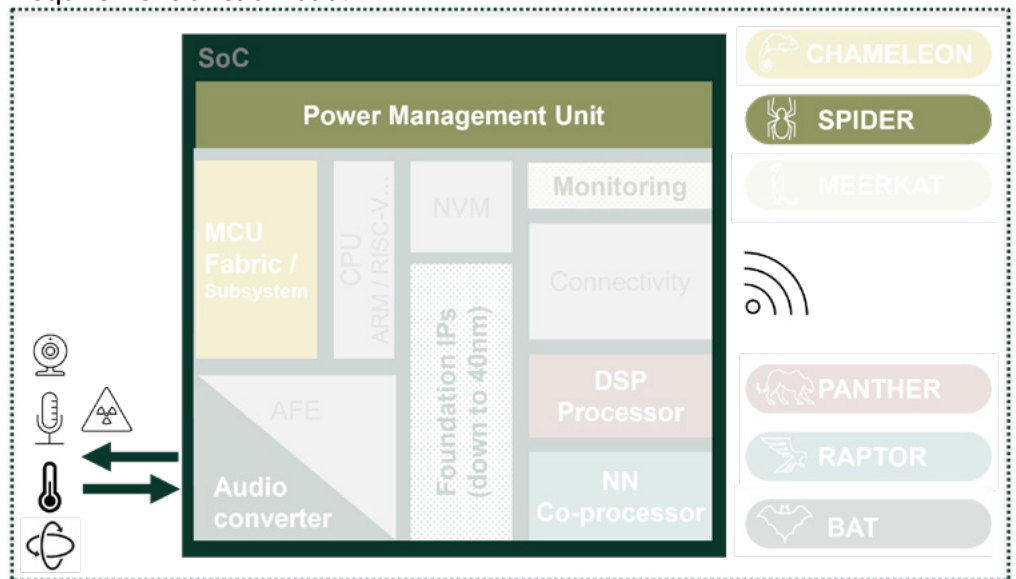
APPLICATIONS

- Audio: TWS, Smart speakers, ...
- Connectivity: WIFI, BLE, Narrow-band IoT, ...
- GNSS
- MCU: High Perf, GP and uLP, ...
- Industrial
- Automotive: Infotainment, TPMS, ...

SPIDER is the most complete Power Management IP platform to speed-up and secure the design of energy-efficient SoCs. It includes all kinds of voltage regulators, low frequency oscillators, voltage monitors... to supply reliably active and always-on power domains of any SoC.

SPIDER also features a configurable digital power controller. It enables to safely control all resources of each power domain (voltage regulator, power gating...). Its unique architecture ensures ultra-fast and autonomous start-up as well as power mode changes.

For ultimate energy efficiency and performance optimization, SPIDER natively supports Adaptive Body Bias and Voltage Scaling.
Silicon IPs part of SPIDER are provided duly configured for the current requirement of each load.

KEY FIGURES

- Supports USB & all battery types from 1.62 to 5.5V input supply voltage
- Flexible configuration from 50mA to 1A
- Embedded ePMU with 500nA sleep current
- More than 150 IPs in product portfolio
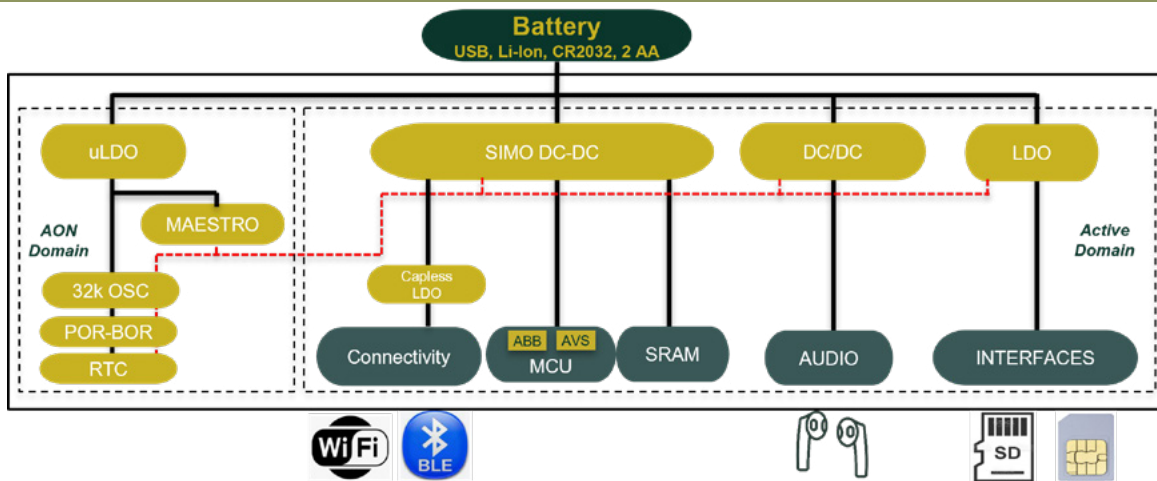- Wide offering from 180 to 12nm process nodes (Bulk, FDSOI & FinFet*)
  under development

TECHNOLOGY FOR BETTER FUTURE

The exponential growth of needs for greater device interoperability, predictability and performances is challenged by the global need for more energy frugality. By 2030, 24B of IoT devices will be battery powered and 5B batteries will be replaced every year (15M units per day!).

This is where SPIDER power management IP platform plays a key role. Through the safe integration of an energy efficient power management network designers can significantly reduce the energy needed to operate their SoC which in turn extends the battery lifespan and limits the volume of toxic materials to be recycled at the battery end-of-life.

Dolphin Design's SPEED IP platform is labelled by the Solar Impulse Foundation among 1,000 solutions for tomorrow.

Example of Power Management network enabled by SPIDER

KEY BENEFITS

- Fast power management integration leadtime in SoC

- Flexible, configurable and secure power management integration in SoC

- SoC energy efficiency and BoM cost optimization

- Enabler for advanced uLP technics integration (Adaptive Body Biasing, Adaptive Voltage Scaling, Power Gating)

KEY FEATURES

- AON in deep sleep mode <500nA

- Input voltage up to 5.5V

- Output voltages from 0.5V to 3.3V with fine grain programmability

- High DC accuracy (3%) with Trimming-less elements

- Configurable output current for any application

- Instant generation of tailored ePMU (RTL and UPF testbench)

- Events manager

SPIDER is a one stop shop IP platform solution matching your needs from standalone IP up to full PMIC integration.

DCDC REGULATORS
High efficiency at high load (90%) and low load (70% @10uA)
Low quiescent current (280nA)
Low BoM (1uH)
Large output current range (from 50mA up to 2A)

SIMO DCDC REGULATORS
4 independent outputs with total current of 400mA
Low BoM with single inductor (1uH)
Fine grain output voltage step (5mV) for DVFS, AVS

LDO REGULATORS
Low quiescent current LDO for AON domain (150nA)
High PSRR LDO (50 dB DC) for noise sensitive blocks
Capless LDO for BoM and pin count saving

POR-BOR
Programmable POR and BOR threshold
Ultra low current consumption in burst mode (< 100nA)

LOW FREQUENCY OSCILLATORS
32kHz RC and XTAL
Low current consumption (<80nA)

MAESTRO ePMU
Configurable digital ePMU IP with PowerStudio toolsuite generating Power Network, ePMU RTL and UPF testbench for fast and secure design of ultra low leakage AON domain

ADAPTATIVE BODY BIASING (ABB) & VOLTAGE SCALING (AVS)
Self-contained and autonomous IP to dynamically compensate Process, Voltage and Temperature variations
Significant PPA gains (> 10x power reduction at 0.5V)
Process agnostic AVS (FDSOI, Bulk, FinFet)

WE TECH IT ON

DOLPHIN
D E S I G N